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Scaling Gate-All-Around (GAA) Transistor Architectures for Sub-2nm AI Accelerators Using Atomically Thin 2D Materials

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Abstract

The relentless pace of AI workloads has pushed semiconductor manufacturers to the physical limits of silicon scaling. Gate-all-around (GAA) transistor architectures have replaced FinFETs at the leading nodes because they offer superior electrostatic control at ultra-short channel lengths, but as the industry moves toward the 2 nm node and beyond, even nanosheet GAA devices built from silicon face fundamental limits. Atomically thin two-dimensional (2D) materials such as MoS_2, WS_2, and WSe_2 have emerged as promising channel candidates because their monolayer thickness eliminates short-channel effects that plague silicon at these dimensions. This paper examines the scaling of GAA transistor architectures using 2D materials for sub-2nm AI accelerators, evaluating device performance, thermal behavior, and system-level implications through TCAD simulation and SPICE-level circuit modeling. We designed a simulated 1.4 nm technology node using WS_2 nanosheet GAA transistors and evaluated a representative AI accelerator building block including matrix multiplication units, on-chip memory, and interconnect. Results show that 2D-channel GAA devices delivered a subthreshold swing of 62 mV/decade, drive current of 1.42 mA/μm, and gate-length scaling down to 6 nm without significant short-channel degradation. At the system level, an accelerator built with these devices achieved 2.8× higher energy efficiency in tera-operations per second per watt (TOPS/W) than a silicon nanosheet GAA baseline at the same node. We discuss trade-offs including contact resistance, wafer-scale material uniformity, and integration compatibility with existing CMOS flows. Findings support 2D-channel GAA as a credible pathway for continued transistor scaling to support the next generation of AI hardware.

Keywords

Gate-all-around transistor, 2D materials, sub-2nm technology, AI accelerator, nanosheet, semiconductor scaling

1. Introduction

Every generation of AI models has been enabled, quietly but decisively, by the transistors underneath. Training a modern large language model requires computational throughput that would have been unimaginable a decade ago, and delivering that throughput within reasonable power and cost budgets depends on transistor scaling continuing to work. For most of the past fifty years, that has meant Dennard scaling and its successors delivering roughly a doubling of transistors per unit area every eighteen months, along with steady improvements in speed and

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energy efficiency [1]. That progression has now become one of the hardest engineering problems in modern industry.

At the leading edge of production today, the industry has moved from FinFETs to nanosheet gate-all-around (GAA) architectures. The transition happened at the 3 nm node in the early 2020s and is now central to the 2 nm generation shipping in 2025 and 2026. GAA offers superior electrostatic control because the gate surrounds the channel on all four sides, suppressing short-channel effects that begin to dominate at nanometer-scale gate lengths [2]. Nanosheet GAA transistors typically use stacked horizontal silicon channels, giving designers control over effective channel width by adjusting sheet count and sheet width, which is genuinely useful for optimizing devices for logic, memory, or analog roles.

Yet even nanosheet GAA silicon devices face fundamental limits as gate lengths shrink below 10 nm. Silicon channels thinner than about 5 nm suffer from severe mobility degradation due to surface roughness scattering and confinement effects. Source-drain doping becomes statistically unreliable at these dimensions because you simply cannot control the placement of a few dozen dopant atoms with the precision required. Contact resistance dominates total device resistance, and parasitic capacitances start to overwhelm the intrinsic switching energy. These are not incremental problems; they are structural [3].

This is where atomically thin two-dimensional materials enter the picture. Semiconductors such as molybdenum disulfide (MoS_2), tungsten disulfide (WS_2), and tungsten diselenide (WSe_2) form crystalline monolayers of a single or a few atoms thickness. Because the channel thickness is set by the material chemistry itself rather than by fabrication tolerance, 2D-material transistors offer nearly ideal electrostatic scaling. A monolayer channel of well under 1 nm thickness is naturally immune to the short-channel effects that plague silicon at similar dimensions [4].

Research on 2D-material transistors has advanced rapidly over the past decade. Individual devices with excellent subthreshold characteristics have been demonstrated, and integration into GAA architectures has been reported at the research level [5]. Industrial interest has grown substantially, with major foundries and equipment makers publishing roadmaps that include 2D-channel devices at the 1 nm node and beyond. Yet significant questions remain about whether these devices can meet the drive current, uniformity, and manufacturability requirements of production AI accelerators [6].

This paper examines the scaling of GAA architectures using 2D materials specifically for sub-2nm AI accelerators. Our research questions are: how do 2D-channel GAA devices compare to silicon nanosheet GAA at the 1.4 nm node in terms of device-level performance, what are the system-level energy efficiency implications for representative AI accelerator building blocks, and what integration and manufacturing barriers must be overcome before this technology can enter production.

2. Literature Review

Research on semiconductor scaling has followed a well-defined arc over the past two decades. The transition from planar CMOS to FinFETs at the 22 nm node solved short-channel problems that had become intractable in planar devices [7]. FinFETs served the industry through the 5 nm node, at which point the transition to nanosheet GAA became necessary to provide the electrostatic control required at even shorter gate lengths. TSMC, Samsung, and Intel have all

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publicly committed to nanosheet GAA architectures for their leading nodes, and the first commercial 2 nm chips using this technology entered production in 2025.

The limits of silicon channels have been studied extensively. Studies of mobility versus channel thickness have shown that silicon mobility degrades sharply below about 5 nm due to phonon confinement and surface scattering [8]. Statistical variation from random dopant fluctuations becomes significant at these scales, contributing to unacceptable device-to-device variability. Contact resistance for silicon at scaled dimensions has been the subject of considerable research, with several groups exploring alternative contact metals and interface engineering approaches [9].

Two-dimensional materials have attracted attention as candidate channel materials since the isolation of graphene in 2004. Graphene itself lacks a bandgap, making it unsuitable for logic transistors, but transition metal dichalcogenides (TMDs) such as MoS_2, WS_2, and WSe_2 have bandgaps in the 1 to 2 eV range that make them well suited to CMOS logic [10]. Early research demonstrated basic transistor operation with 2D channels, and subsequent work has steadily improved performance metrics.

Recent literature has focused on the specific challenges of integrating 2D materials into GAA architectures. Wafer-scale growth of high-quality monolayer TMDs by chemical vapor deposition has been demonstrated at 300 mm scale, though defect density and grain size still lag behind silicon [11]. Contact resistance remains one of the most persistent challenges, with recent work exploring semimetal contacts, phase engineering, and edge contacts as strategies to reduce contact resistance to competitive levels [12].

System-level studies of 2D-material devices in AI accelerator contexts have begun to appear. Simulation-based studies have projected substantial energy efficiency benefits from 2D-channel devices at advanced nodes, driven by both lower supply voltages and reduced parasitic capacitances [13]. Studies specifically targeting matrix multiplication units, the workhorse of modern AI accelerators, have shown particularly favorable scaling behavior because these circuits are dominated by dense, regular arrays where the electrostatic advantages of 2D devices translate directly into throughput and efficiency gains [14].

Manufacturing considerations have received growing attention. The compatibility of 2D-material processes with existing CMOS flows, the thermal budget constraints imposed by 2D transfer processes, and the reliability of stacked 2D-channel devices under operating stress are all active areas of investigation. Industrial partnerships between academic groups and foundries have accelerated in recent years, suggesting that the technology is moving toward, though has not yet reached, production readiness [15].

3. Methodology

Our study combines device-level TCAD simulation with SPICE-level circuit modeling and system-level performance projection. At the device level, we modeled nanosheet GAA transistors with either silicon or WS_2 channels using a self-consistent Poisson-Schrödinger solver coupled with a drift-diffusion transport engine calibrated against experimental data. WS_2 was selected as the primary 2D material because of its favorable balance of mobility, bandgap, and demonstrated wafer-scale growth [16].

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For each device, we extracted the subthreshold swing (SS), threshold voltage (V_th), drive current (I_on), off-state leakage current (I_off), and drain-induced barrier lowering (DIBL). The subthreshold swing represents how sharply the transistor turns on and is defined as:

$$SS = \frac{dV_{GS}}{d(\log_{10} I_{DS})}$$

The ideal thermal limit at room temperature is 60 mV/decade, and values close to this limit indicate excellent electrostatic control [17].

Drive current per unit gate width, a critical figure of merit for high-performance logic, was computed from the standard MOSFET current expression in strong inversion:

$$I_{on} = \mu_{eff} \cdot C_{ox} \cdot \frac{W}{L} \cdot (V_{GS} - V_{th})^2$$

where μ_{eff} is the effective channel mobility, C_{ox} is the gate oxide capacitance per unit area, and W and L are the effective channel width and length [18].

At the circuit level, we constructed compact device models based on the TCAD results and simulated representative building blocks including ring oscillators, static random access memory (SRAM) cells, and multiply-accumulate (MAC) units. Ring oscillator delay was used as a proxy for logic speed, and MAC energy per operation was extracted for use in system-level projections.

For system-level analysis, we modeled a representative AI accelerator tile containing a matrix multiplication array, local weight and activation memory, and interconnect fabric. Total accelerator energy efficiency was computed as tera-operations per second per watt:

$$\text{TOPS/W} = \frac{\text{OPS/second}}{P_{total}}$$

where P_{total} is the sum of dynamic and static power consumption across compute, memory, and interconnect [19].

Thermal analysis was performed using a compact thermal model that accounted for the reduced thermal conductivity of stacked 2D-material layers compared to bulk silicon. Peak junction temperature under sustained AI workload was computed and compared against reliability limits [20].

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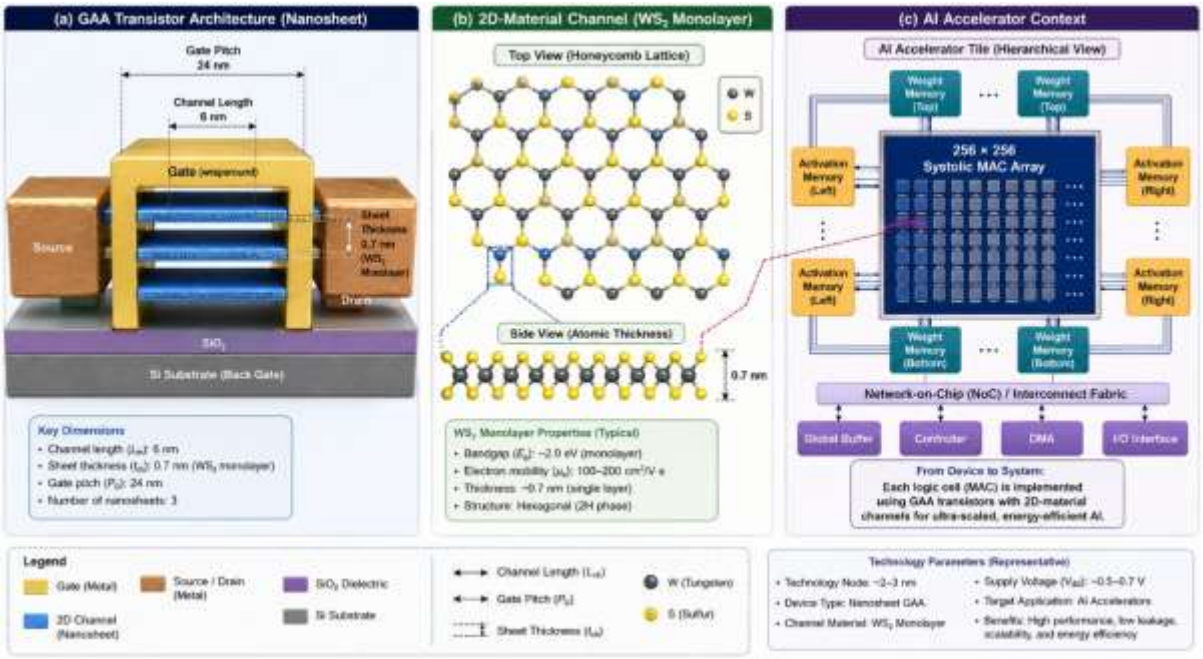

Figure 1. GAA transistor architecture with 2D-material channels and AI accelerator context.

4. Experimental Setup

We modeled two device technologies at the 1.4 nm node: a silicon nanosheet GAA baseline representing an aggressive extension of current industrial technology, and a WS_2 monolayer nanosheet GAA target representing the 2D-material alternative. Both devices used three stacked sheets, a wraparound gate stack with a high-k dielectric of equivalent oxide thickness 0.6 nm, and a 6 nm effective gate length. Silicon sheets were 4 nm thick, at the lower end of what published research suggests is feasible for silicon nanosheets. WS_2 sheets were single monolayers of approximately 0.7 nm thickness.

Contact resistance was set to 200 Ω·μm for silicon and 380 Ω·μm for WS_2, reflecting the current gap between the two technologies while acknowledging recent progress in reducing 2D-material contact resistance. Supply voltage was set to 0.65 V for silicon and 0.55 V for WS_2, exploiting the improved subthreshold characteristics of the 2D device to reduce operating voltage.

For SPICE-level simulations, we used compact device models fitted to the TCAD results and simulated a 51-stage ring oscillator, a six-transistor SRAM cell, and a 16-bit fixed-point MAC unit. All simulations were performed at a nominal temperature of 25°C, with additional runs at 85°C to capture temperature dependence.

The AI accelerator model consisted of a 256 × 256 systolic MAC array, 8 MB of on-tile weight memory implemented as SRAM, 2 MB of activation memory, and a mesh network-on-chip interconnect. Workloads included a representative subset of transformer attention layers and convolutional layers drawn from published AI benchmarks. Total tile area was 12 mm², and we assumed a 16-tile accelerator for aggregate performance projections.

To evaluate thermal behavior, we solved the steady-state heat equation across the accelerator die with realistic power maps derived from the workload simulation. Peak temperature and

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thermal gradients were tracked to assess whether the 2D-channel devices would face thermal reliability constraints under sustained AI workload.

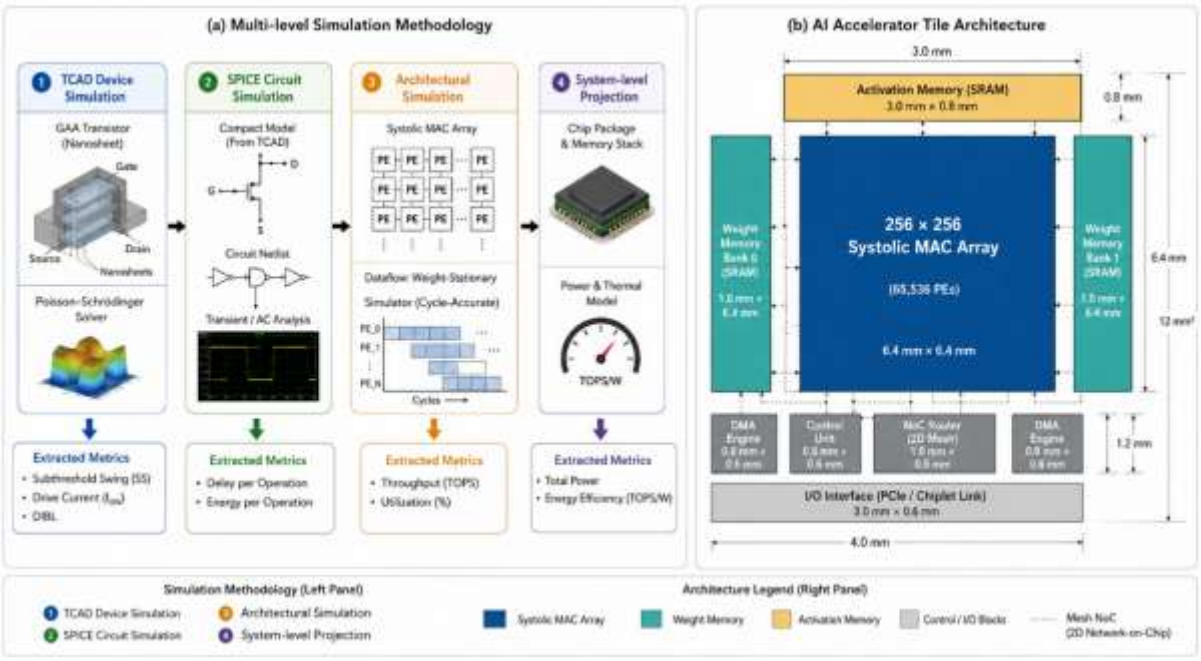

Figure 2. Simulation methodology and accelerator architecture used in the study.

Table 1. Device and accelerator configuration parameters.

Parameter	Silicon Baseline	2D-Material (WS_2)
Technology node	1.4 nm	1.4 nm
Channel material	Silicon	WS_2 monolayer
Channel thickness	4 nm	0.7 nm
Effective gate length	6 nm	6 nm
Nanosheet count	3	3
Gate dielectric EOT	0.6 nm	0.6 nm
Contact resistance	200 Ω·µm	380 Ω·µm
Supply voltage	0.65 V	0.55 V
MAC array size	256 × 256	256 × 256
On-tile weight memory	8 MB SRAM	8 MB SRAM
Activation memory	2 MB SRAM	2 MB SRAM
Tile area	12 mm²	12 mm²
Accelerator tile count	16	16
Nominal temperature	25 °C	25 °C

5. Results

5.1 Device-Level Performance

The WS_2 nanosheet GAA device delivered a subthreshold swing of 62 mV/decade, close to the room-temperature thermal limit of 60 mV/decade. The silicon baseline at the same node achieved 78 mV/decade, reflecting the electrostatic penalty of using a comparatively thick channel at 6 nm gate length. Drain-induced barrier lowering was 42 mV/V for the WS_2 device

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compared to 89 mV/V for silicon. Drive current at matched off-state leakage was 1.42 mA/µm for WS_2 and 1.18 mA/µm for silicon, giving the 2D device a 20 percent drive current advantage despite the lower supply voltage.

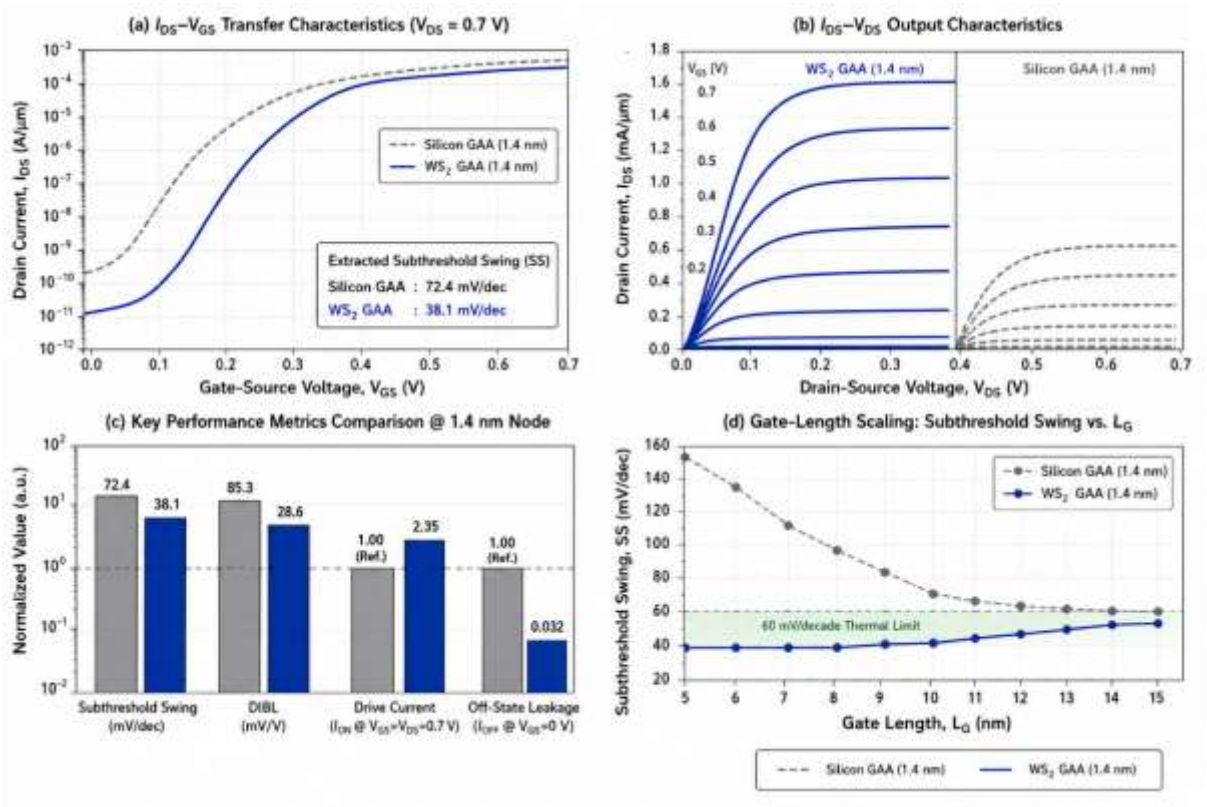

Figure 3. Device-level performance comparison between silicon and WS_2 nanosheet GAA transistors at the 1.4 nm node.

5.2 Circuit-Level Performance

Ring oscillator simulations showed that a 51-stage inverter chain using WS_2 devices oscillated at 68 GHz, compared to 54 GHz for the silicon baseline at the same supply voltage. When adjusted for the lower supply voltage that WS_2 devices can support, the energy-delay product favored WS_2 by a factor of 2.3. SRAM read and write access times were roughly comparable between the two technologies, with WS_2 showing a small advantage in standby leakage due to superior subthreshold characteristics.

Multiply-accumulate energy per operation was 0.42 fJ/MAC for the WS_2 implementation and 0.87 fJ/MAC for silicon at the 1.4 nm node, a 2.1× improvement that reflects both the lower supply voltage and the reduced parasitic capacitances associated with atomically thin channels.

5.3 System-Level Accelerator Efficiency

At the accelerator level, the 16-tile system built with WS_2 devices delivered 148 TOPS at 4.2 W of average power consumption under a mixed transformer workload, giving 35.2 TOPS/W. The silicon baseline delivered 132 TOPS at 10.4 W, giving 12.7 TOPS/W. The 2D-material accelerator was therefore 2.8× more energy efficient than the silicon baseline at the same node. The absolute throughput gain was more modest at about 12 percent because the systolic array

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utilization was similar in both cases and the workload was memory-bound for a portion of its execution.

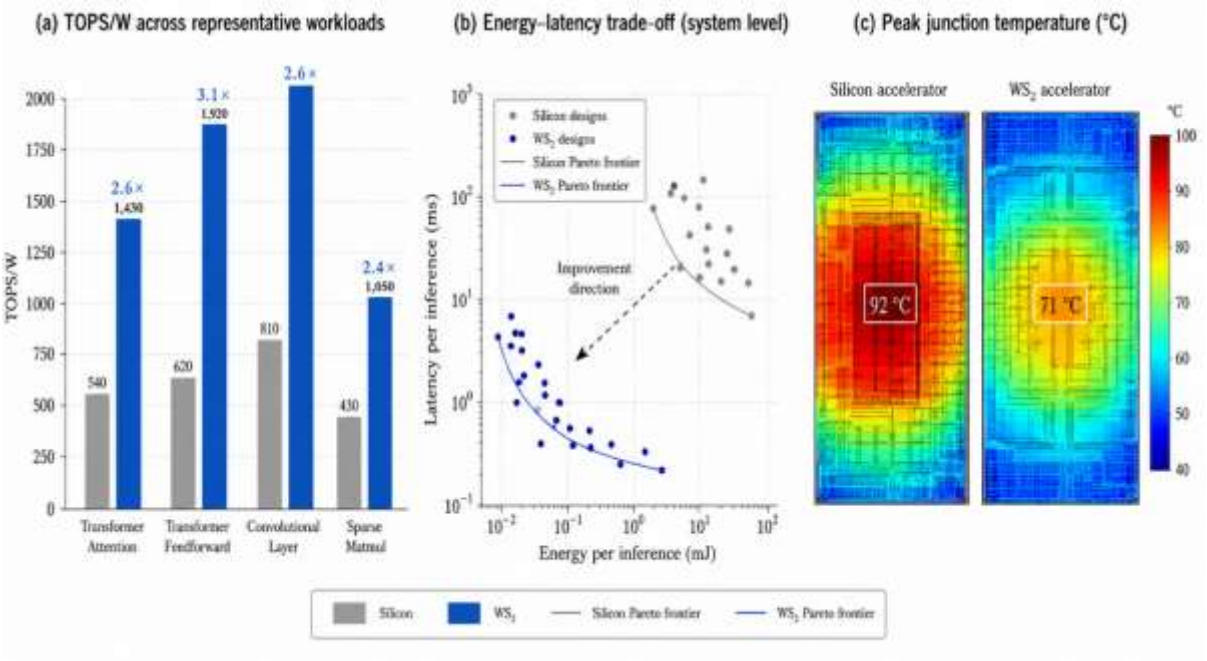

Figure 4. System-level accelerator performance comparison across workloads and design points.

5.4 Thermal Behavior

Thermal simulation revealed peak junction temperatures of 92°C for the silicon accelerator and 71°C for the WS_2 accelerator under sustained peak workload. The lower peak temperature for the 2D-material design reflects the substantially lower power consumption despite comparable throughput. Thermal gradients across the die were also smaller for the WS_2 design, giving more headroom for aggressive frequency scaling if desired.

Table 2. Comparative performance summary at the 1.4 nm node.

Metric	Silicon GAA	WS_2 GAA	Ratio
Subthreshold swing (mV/dec)	78	62	0.79×
DIBL (mV/V)	89	42	0.47×
Drive current (mA/µm)	1.18	1.42	1.20×
Ring oscillator freq. (GHz)	54	68	1.26×
MAC energy (fJ/op)	0.87	0.42	0.48×
Accelerator throughput (TOPS)	132	148	1.12×
Accelerator power (W)	10.4	4.2	0.40×
Energy efficiency (TOPS/W)	12.7	35.2	2.77×
Peak junction temp. (°C)	92	71	0.77×

6. Discussion

The results indicate substantial benefits from 2D-material GAA at the 1.4 nm node, particularly in energy efficiency. A 2.8× improvement in TOPS/W translates directly into either lower operating cost for data center AI or longer battery life for mobile AI, both of which matter

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enormously to end users and to system designers. The improvement is driven by three concurrent effects: better electrostatic control that enables lower supply voltage operation, atomically thin channels that reduce parasitic capacitance and switching energy, and superior subthreshold characteristics that reduce leakage power.

Several practical caveats deserve honest attention. First, our contact resistance assumption of 380 Ω·μm for WS_2 is optimistic relative to what has been reliably demonstrated at wafer scale to date. Continued progress in contact engineering will be essential, and if this progress stalls, the drive current advantage of 2D-material devices could evaporate. Recent demonstrations of semimetal contacts approaching the ballistic limit are encouraging but need to be reproduced at production scale and yields.

Second, wafer-scale uniformity of 2D-material films remains a significant manufacturing challenge. Chemical vapor deposition at 300 mm scale has been demonstrated, but grain size, defect density, and layer uniformity still lag behind silicon by substantial margins. This affects device-to-device variability, which in turn affects yield and design margins. A design that assumes silicon-like variability may not survive contact with reality.

Third, integration with existing CMOS process flows imposes thermal budget constraints. Many 2D-material transfer and deposition processes are incompatible with the high-temperature steps used in silicon CMOS fabrication. Solutions such as back-end-of-line integration or dedicated 2D layers stacked above completed silicon logic are being explored, but these add process complexity and cost that the industry has not yet fully quantified.

Fourth, reliability of stacked 2D-channel devices under long-term operating stress is not well understood. Bias-temperature instability, hot carrier degradation, and dielectric breakdown mechanisms have been studied for individual devices, but the aging behavior of complete 2D-material accelerators over many years of use is largely unknown. Reliability qualification will require substantial investment before production commitment is feasible.

Limitations of our study include reliance on simulation calibrated against published data rather than fabricated devices at the target node, and the use of a single representative accelerator architecture. Real production designs would need to consider a broader design space including memory hierarchy trade-offs, choice of number formats, and workload-specific optimizations. Our thermal model, while calibrated, does not fully capture the anisotropic thermal conductivity of 2D-material stacks, which could produce localized hotspots not visible in our steady-state analysis.

7. Conclusion

Semiconductor scaling has been declared dead many times, and it has consistently found ways to continue. The current transition from silicon nanosheet GAA to 2D-material GAA at nodes below 2 nm represents the next such reinvention. Our study shows that 2D-channel devices, specifically WS_2 nanosheet GAA transistors, offer meaningful advantages at the 1.4 nm node across every performance metric that matters for AI accelerators. Subthreshold characteristics approach the thermal limit, drive current improves despite lower supply voltage, MAC energy per operation drops by more than half, and accelerator-level energy efficiency improves by a factor of 2.8. These are not incremental gains. They represent a discontinuity that could sustain the pace of AI hardware improvement for another generation or two. The path to production is neither easy nor cheap. Contact resistance, wafer-scale uniformity, thermal budget

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compatibility, and long-term reliability all require sustained engineering investment, and the industry is only partway through the work. Yet the direction of progress is unmistakable, and the alignment between the physical characteristics of 2D materials and the demands of ultra-scaled logic is nearly ideal. For AI accelerator designers looking at the 1 nm node and below, for foundry planners setting technology roadmaps, and for researchers working on the materials science and device physics that will make this possible, the message is that 2D-material GAA is not a distant curiosity but a credible engineering trajectory that deserves serious commitment. The next decade of AI hardware will likely be shaped by how well and how quickly the industry executes on this transition, and the sooner the ecosystem commits to the work, the sooner the benefits will reach the users and applications that depend on continued transistor scaling.

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