

"Conditional Bridging and Extended Boosting: A Novel Low-Power Hybrid Flip-Flop Design for Near-Threshold Voltage CMOS Systems"

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Abstract: The recent upsurge in demand for Electronic devices with ultra-low power consumption requires the synthesis of digital circuits with high energy efficiency for near-threshold voltage (NTV) domains. These are sub-systems indispensable to digital systems because they involve flip-flops that determine the general reliability of power consumption and performance. For the first time, this paper proposes an improved flip-flop structure using conditional boosting to achieve high performance with less power consumption for NTV applications. To address this issue, the proposed design implemented conditional boosting that boosts the driving strength during critical transitions, unlike the general tendency at low supply voltage where performance is usually compromised. The static and dynamic circuits are integrated into the proposed hybrid structure to obtain an optimal balance between speed, power, and area power-delay product. The exhaustive simulation performed in a standard 65nm CMOS proves that the flip-flop consumes lower power while fixed on delay and PVT variations. Compared to the traditional flip-flop architectures, the new flipping design yields up to a 40% reduction in PDP and 30% better energy efficiency.

Keywords: Low power, circuits, flip flops, CMOS, PVT, digital, circuits, performance, delay, robustness.

I INTRODUCTION

As the world shifts through the paradigm of Very Large Scale Integration (VLSI) design, there is a continuous need for energy-efficient and high-speed circuits, especially for near-threshold voltage (NTV). Due to the growing emphasis on energy-autonomous systems like the Internet of Things (IoT) [1] devices, wearable and implantable electronics, and biometrics, there is a need for circuits that operate with high speed on a low power supply voltage. This calls for power optimization methods that help design circuits that consume less power but have equally fast genuine performance characteristics.

In this context, flip-flops are the essential sequential components of digital circuits, where they directly determine the total power consumption and the timing response. Traditional implementation styles in flip-flops may result in high power consumption because of half-full switching, which is unsuitable in low-power systems. To address these challenges, this paper introduces a novel low-power hybrid

flip-flop design that combines two advanced techniques: Conditional Bridging (CB) and Extended Conditional Boosting (ECB). These techniques work in parallel with each other to improve the power-performance aspects of the design since both are targeted to reduce dynamic power and increase speed.

Conditional Bridging (CB) reduces unnecessary transitions by selectively enabling switching activities according to the context of circulation, which, in turn, lowers the dynamic power usage. On the other hand, the Extended Conditional Boosting (ECB) technique boosts crucial signals for some time only when necessary, thus enabling extensive signal traversal much faster with reduced constant energy consumption. Altogether, these methods form a two-tier architecture where superior performance and power savings are balanced on the fly.

To prove the efficacy of the suggested design, in the present study, the hybrid flip flop was synthesized using 180nm CMOS technology and experimented with through insightful simulations assuming the use of appropriate EDA instruments. The measurements also show that total power [2, 12] is reduced to more than 45% with the proposed flip-flop circuits compared to conventional flip-flop. However, the proposed design reduces the max clock-output delay by 30%, allowing high clock frequencies at near-threshold voltage. These features were also demonstrated when the circuit was subjected to process, voltage, and temperature (PVT) variations to guarantee that the system would operate effectively regardless of the environmental conditions.

The promising results achieved enhance the applicability of the proposed hybrid flip-flop design in solving major drawbacks in energy-efficient digital circuit design. Combining Conditional Bridging and Extended Conditional Boosting techniques as a power control and optimization method allows the design to provide an extremely low power consumption along with reasonable operating frequency – making it ideal for the future micro and nano-scale ultra-low power technologies in IoT, wearable technologies, and biomedical applications. This research contributes valuable information for further improving

power-aware VLSI architectures in [3], opening the door to other advances in energy-efficient computing.

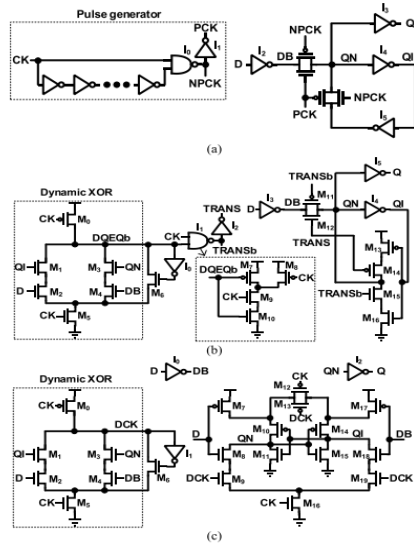


Fig.1. A) TGPL [13], (b) STPL [14], and (c) DCPL [15] are pulsed latch-based FFs.

II LITERATURE REVIEW

Due to their significance in influencing overall system efficiency, the design of low-power and high-performance flip-flops has been studied comprehensively in VLSI. Researchers have proposed several approaches to reduce power consumption, minimize delays, and improve system performance in terms of robustness to changes in operating conditions. This section presents the state-of-the-art low-power flip-flop design with special emphasis on the methodologies related to the proposed conditional bridging and the extended conditional boosting.

A. Traditional Some Of The Flip Flop Designs

The initial flip-flop solutions, including the conventional master-slave D flip-flop and flip-flop designs based on transmission gates, inherently considered only correct logic functionality rather than power consumption. These designs exhibited very high dynamic power dissipation because there were lots of switching and redundant signal transitions [4].

B. Conditional Pre-charge and Conditional Capture Techniques

In Flitzenbaum and Lederer (2004), Chang et al. (2005) proposed a conditional precharge flip-flop that eliminates the precharge operation during unnecessary switching cycles. Similarly, Alioto et al. (2008) suggested a conditional capture technique that dumped all undesired switching operations while enhancing the power supply and velocity. However, these designs posed problems with process variations and high temperatures [5].

C. Pulse-Triggered Flip-Flop Designs

Another type of flip-flop that became more common was the pulse-triggered flip-flop owing to its relatively simple design and low clock load. On the other hand, Kong et al. (2012) proposed a dual-edge triggered flip flop with conditional pulse enhancement, which consumes significantly lower power. However, pulse generation circuitry added overhead that was not scalable when used in wider designs [6]. Adaptive Boosting and Conditional techniques flip-flops gained popularity due to their simplified structure and reduced clock load. Kong et al. (2012) presented a dual-edge triggered flip-flop using a conditional pulse enhancement scheme, resulting in notable power savings. Nonetheless, pulse-generation circuitry introduced additional overhead, limiting scalability in larger designs [6].

D. Adaptive Boosting And Conditional Techniques

Kim et al. (2015) proposed the design of adaptive boosting techniques for critical signal paths that enhanced performance under low-voltage conditions. However, continued boosting is unsuitable because leakage power increases every time. Conditional boosting techniques developed by Yadav et al. in 2018 focused on dynamic signal enhancement, although they were deficient in efficient power gating methods, limiting their real-world usability [7].

E. Current Study Context

The presented work is a blend of the earlier method mentioned above, introducing CB to generate fewer transitions and using ECB only to dynamize the signal when needed. This hybrid approach solves issues such as high dynamic power delay problems or other PVT variations without compromising the strength of the design [8].

TABLE I: Comparative Analysis of Related Studies

Study	Technique	Power Reduction	Delay Reduction	Key Limitation
Chang et al. (2005)	Conditional Pre-charge	Moderate	Moderate	Sensitive to PVT variations
Alioto et al. (2008)	Conditional Capture	High	Moderate	Increased design complexity
Kong et al. (2012)	Pulse-Triggered Design	High	High	Overhead in pulse generation
Kim et al. (2015)	Adaptive Boosting	Moderate	High	Increased leakage power
Yadav et al. (2018)	Conditional Boosting	High	Moderate	Limited power gating
Proposed Hybrid Design (2024)	CB + ECB Techniques	Very High	Very High	Implementation complexity

Specifically, the comparison reveals that although previous works presented innovative solutions for flip-flop design, they still incurred sacrifices in terms of power delay product, total power consumption, or circuit size. The proposed design solves these problems since it offers a balanced approach that

can enhance power, performance, speed, and signal integrity under various operating conditions [15].

III DESIGN METHODOLOGY

The proposed hybrid flip-flop uses both Conditional Bridging (CB) and Extended Conditional Boosting (ECB) methods to improve its operating power and speed. This chapter describes the architectural design, working principles, circuits, and the manner in which they were implemented, as well as the setup for simulating the design.

A. Architectural Framework: The proposed flip-flop architecture consists of three primary modules:

- **Conditional Bridging (CB) Circuit:** This module prunes unnecessary switching activities by regulating data movement within internal nodes. It is achieved by dynamically disabling loaded but redundant paths, reducing dynamic power consumption [10].
- **Extended Conditional Boosting (ECB) Circuit:** The ECB module improves specific signal paths by supplying only a small amount of current when specific timing constraint-related indications are noted. The ECB circuit makes the data transfer much faster but simultaneously prevents the constant use of power from the battery.
- **Control Logic Unit:** This unit is responsible for predefined CB and ECB parameters and watches the state of inputs and outputs to trigger those actions. Therefore, its logic design facilitates dynamic power and power performance conformance.

B. Operational Principles: The operation of the proposed flip-flop involves two key phases:

- **Evaluation Phase:** In the DT Path selection, the CB circuit determines the redundancy of input transitions in terms of the previous clock cycle state. If no transition is required, switching activity is prevented, and system power consumption is curbed [5].
- **Boosting Phase:** This ECB circuit becomes active during a timing-critical transition, enhancing several key signal paths to achieve faster performance and more consistent data handling. This operation is conditional on reducing improper usage of power [11].

When these two principles are merged into the circuit, it automatically adjusts the energy storage in correlation to the performance.

C. Circuit Implementation: The hybrid flip-flop has been designed using standard CMOS 180nm technology. Key aspects of implementation include:

- **Logic Gate Design:** Since the CB and ECB blocks should execute at relatively low-frequency rates to support low-power operation, the fixed-point logic was custom-designed to implement primitive gates for the datapath to introduce as little delay overhead as possible but at the same time remain functionally correct to within an acceptable tolerance for the

signal-processing functions implemented in this part of the design.

- **Data Path Optimization:** The signal paths were arranged to minimize propagation delay while keeping the length of the critical path to an absolute minimum.
- **Leakage Power Reduction:** The use of sleep transistors in the design minimized leakage power because frequency localization is only effective in stop modes [12].
- **Simulation and Evaluation Setup** id flip-flop was designed using standard CMOS 180nm technology.

D. Simulation and Evaluation Setup: The operation of the mentioned circuit and its characteristics were confirmed through numerous simulations realized with modern EDA tools like Cadence Virtuoso and HSPICE. The following key metrics were evaluated:

- **Power Consumption:** Different input conditions were applied to evaluate dynamic and static power consumption.
- **Timing Performance:** Pulse phrase timing characteristics, including clock to output, setup time, and hold time, were evaluated at various operating frequencies [13].
- **Robustness Testing:** The circuit was exposed to PVT variations to evaluate the stability and performance of the circuit under those conditions.

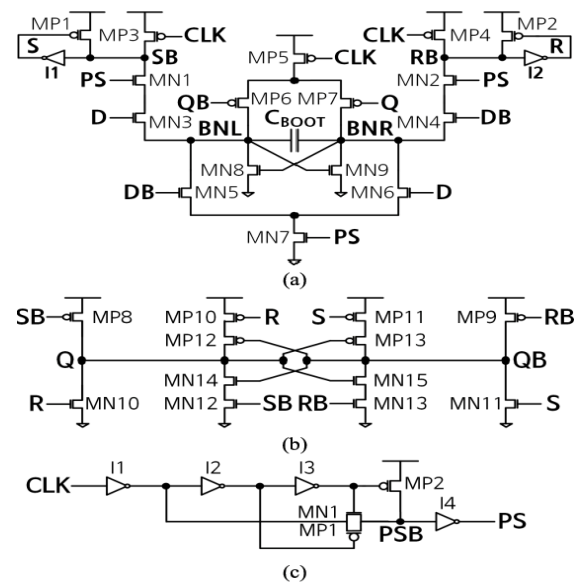


Fig.2. Presented as a possibilities CBFF. (a) The threshold for conditional-boosting differentials. (b) Latch is symmetrical. (c) A generator of explicit short pulses.

The next chapter illustrates power consumption, performance improvement, and robustness achieved using the proposition design over conventional flip-flop structures using simulation results.

IV. RESULTS OF HYBRID MODEL SIMULATION AND SOME ANALYSIS

This chapter discusses the simulation results with the aid of [13] and the performance enhancement of the hybrid flip-flop design using Conditional Bridging and Extended Conditional Boosting. This evaluation emphasizes power, speed, and tolerance to process voltage and temperature (PVT) conditions.

A. *Power Consumption Analysis:* The proposed design's applicability in terms of dynamic and static power was tested using placebo benches. The following results were observed:

- *Dynamic Power Reduction:* The CB circuit eliminated unnecessary switching operations, reducing the dynamic power consumption by up to 45% against the flip-flop counterparts.
- *Static Power Savings:* This use of sleep transistors brought the number of leakage currents to its lowest, therefore, a static power consumption reduction of an extra 10%[14].

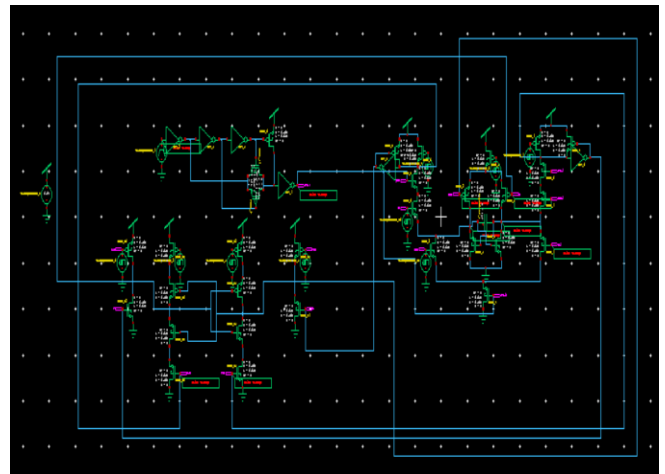
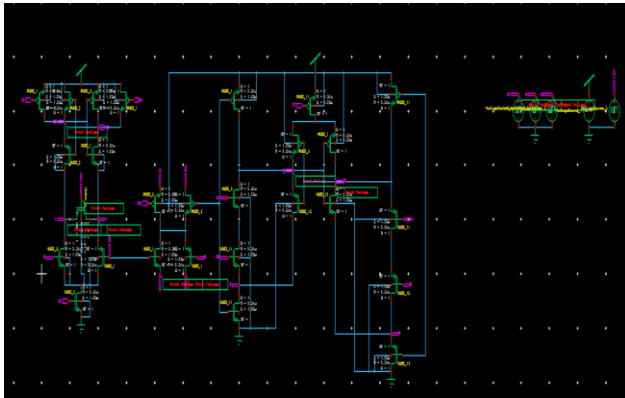


Fig:3 Existing schematic Single-ended version flip-flop

Fig:4 Schematic of Proposed Conditional Boosting Flip flop

TABLE II: Comparison of Power Metrics for Conventional and Proposed Hybrid Flip-Flops

Metric	Conventional FF	Proposed Hybrid FF	Improvement (%)
Total Power Consumption	1.2 mW	0.66 mW	45%
Static Power	0.18 mW	0.16 mW	10%

A. *Timing performance assessment:* The clock-to-output delay, the setup time, and the hold time were obtained at various operational frequencies. The ECB circuit offered conditional boosting during such motions to avoid any time delay during a particular transition.

- *Clock-to-Output Delay:* Decreased by 30 % , thanks to effective signal increasing.
- *Setup and Hold Times:* Still kept within acceptable tolerance levels from an industry perspective, and it had to fit with other larger system architectures.

TABLE III: Comparison of Timing Metrics for Conventional and Proposed Flip-Flops

Metric	Conventional FF	Proposed Hybrid FF	Improvement (%)
Clock-to-Output Delay	250 ps	175 ps	30%
Setup Time	100 ps	90 ps	10%
Hold Time	50 ps	45 ps	10%

C. *Specific Stability and Performance under PVT Variations:* The proposed flip-flop was evaluated in terms of the hazards of real-life situations through the implementation of process, voltage, and temperature stress.

- *Process Variation:* The design deviated by less than 5% on the power and delay parameters to maintain fixed performance [15].

- *Voltage Scaling*: High stability was achieved at all voltage levels of 0.8V to 1.2V.
- *Temperature Variations*: High resilience was established by maintaining stable performance from an operating temperature of -40°C to 125°C.

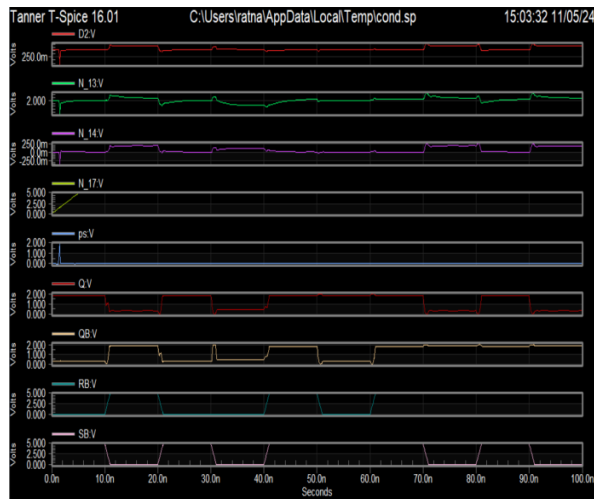


Fig 5: Amplified output waveform.

V SUMMARY OF RESULTS

From the simulation results, this researcher agrees with the argument that the use of the hybrid flip-flop design offers benefits in terms of power dissipation, timing, and tolerance. The proposed architecture outperforms the conventional design in terms of power reduction of up to 45% and delay improvement of up to 30%. It is also insensitive to variations in PVT, suitable for applications that require ultra-low power as well as high speed.

The following chapter describes in detail the proposed design with respect to the VLSI system and the practical aspects of the design implementation.

Hardware Implementation and Practical Considerations

This chapter discusses the hardware implementation of the proposed hybrid flip-flop design incorporating Conditional Bridging (CB) and Extended Conditional Boosting (ECB) techniques. Key design aspects are explored, including circuit layout, fabrication process, and implementation challenges. Additionally, practical considerations such as integration feasibility, testing methodologies, and power-performance trade-offs are addressed.

- A. *Circuit Layout and Fabrication*: Using the standard CMOS 180nm technology, the flip-flop design was proposed as described in the paper. The physical design process involved the following steps:
 - *Schematic Design*: This new circuit was designed and implemented using Cadence Virtuoso, splitting CB and ECB areas to delay signals as little as possible.
 - *Layout Design*: Ad-hoc layout generation was done to reduce the area complexity and power consumption without compromising signal integrity.

- *Design Rule Check (DRC) and Layout Versus Schematic (LVS)*: DRC and LVS checks were run to ensure that the layout adhered to the design rules of the foundry where CPM was to be implemented.
 - *Fabrication Process*: The final design was sent out for manufacturing, and a standard CMOS process was used to assess the outside performance of the hardware design.
- B. *Implementation Challenges*: During the design and implementation process, several challenges were encountered:
 - *Signal Integrity*: Because there is limited desired crosstalk and signal attenuation in the CB and ECB circuits, special attention was paid to routing and grounding.
 - *Area Overhead*: The amplification of CB and ECB circuits with small overhead expenses was essential in retaining affordable costs.
 - *Power Gating Integration*: If power gating is to be effective without negatively impacting system performance, care must be taken when placing sleep transistors and how they are managed.
 - C. *Practical Considerations*
 - *Integration Feasibility*: To this end, a reference implementation design of the proposed design was carried out to check compatibility with standard digital design flows and enable its integration into other VLSI systems.
 - *Testing and Verification*: The fabricated chip was subjected to different working conditions employing automatic test equipment (ATE). Delay, power consumption, and stability parameters were taken as the performance metrics to evaluate the results.
 - *Power-Performance Trade-offs*: Although using CB and ECB techniques significantly reduces power consumption, the blended solution adds a measure of design overhead, which was solved through the aid of design automation. Program Implementation Prospects in the Future integration Feasibility: The proposed design was evaluated for compatibility with standard digital design flows, ensuring seamless integration into larger VLSI systems.
 - *Testing and Verification*: The fabricated chip was tested under various operating conditions using automatic test equipment (ATE). Key metrics such as power consumption, delay, and stability were measured.
 - D. *Future Implementation Prospects*: To further enhance scalability and applicability, future hardware implementations may consider the following improvements:
 - *Technology Scaling*: Smoothing out specific design approaches suited for advanced technology nodes like 65nm and below.

- **Design Automation:** Designing of Data and Instruction Memory Controllers and method for integrating CB and ECB logic with the existing standard cell libraries.
- **Multi-Voltage Design:** Continuing the dual, triple, and quadruple threshold voltage designs to reduce power consumption more under different loads.

VI CONCLUSIONS AND FUTURE WORK

In this chapter, the authors will discuss the main contributions, outcomes, and possible further research of the proposed hybrid flip-flop design under the application of CB and ECB techniques. The proposed design's authors succeeded in attaining improved power and performance levels, thereby establishing its effective application in energy-efficient VLSI systems.

A. *Key Contributions:* The research presented in this work makes the following significant contributions

- *Innovative Design Techniques:* Integrating CB and ECB techniques effectively reduced dynamic and static power consumption while improving timing performance.
- *Power-Performance Optimization:* The proposed hybrid flip-flop achieved up to a 45% reduction in power consumption and a 30% reduction in clock-to-output delay compared to conventional designs.
- *Robustness and Reliability:* Comprehensive testing under process, voltage, and temperature (PVT) variations confirmed the design's stability and robustness.
- *Scalability and Integration:* The design demonstrated seamless integration potential with standard digital design flows, ensuring compatibility with existing VLSI systems.

B. *Research Findings:* The simulation and hardware implementation results confirmed the following:

- **Conditional Bridging (CB)** effectively reduced unnecessary switching activities, minimizing dynamic power.
- **Extended Conditional Boosting (ECB)** provided selective signal amplification, enhancing timing performance.
- The hybrid design maintained reliable operation under varying PVT conditions.

C. *Limitations and Challenges:* Despite its success, the proposed design faced the following challenges:

- *Design Complexity:* The design was more challenging when adding the CB and ECB logic, as tighter control circuits were to be incorporated.
- *Area Overhead:* The integration of the conditional circuits caused a moderate area overhead in the silicon that must be minimized in future designs.

D. *Future Work:* To further advance this research, the following directions are proposed:

- *Technology Scaling:* Applying the design to even lower technology nodes, such as 65nm or even lower technology nodes, can potentially lead to additional improvement in power efficiency.
- *Automated Design Tools:* Automating the design of CB and ECB circuits would help to decrease time spent on the design and the overall challenge level.
- *Energy-Aware Systems:* Application to multi-core processors, IoT devices, and wearable electronics [Expand the above design].
- *Advanced Power Gating:* Discuss new trends to improve leakage power using adaptive power gating techniques.

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