FPGA-BASED COSTAS LOOP DESIGN FOR EFFICIENT BPSK DEMODULATION UNDER DOPPLER EFFECTS

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Abstract. This paper aims to design a resource-efficient demodulator for BPSK-modulated data affected by Doppler shift in the presence of additive white Gaussian noise. The approach involves developing an Automatic Gain Control (AGC) module and a fully digital continuous-mode Costa loop, implemented in XILINX and later converted into VERILOG. The XILINX code is written in fixed-point format to facilitate seamless conversion to VERILOG without complex transformations. The proposed design is simulated using XILINX and Modelsim SE, with performance evaluated through multiple simulations at varying signal-to-noise ratios (SNR) and Doppler frequencies. Simulation results indicate that the demodulator can effectively track frequency offsets up to 20% of the sampling frequency. The proposed design offers significant advantages, including efficient hardware resource utilization, a wide frequency capture range, and high tracking speed. These characteristics make it a suitable solution for communication systems requiring robust demodulation under dynamic conditions.

Keywords: BPSK demodulator; Costas Loop; Doppler frequency; NCO

1 Introduction

Satellites employ diverse modulation schemes with varying data rates, necessitating enhanced flexibility and programmability in ground station demodulators to support multi-satellite data acquisition. Traditional analog circuits have long established and well-understood demodulation techniques for Binary Phase Shift Keying (BPSK) and Quadrature Phase Shift Keying (QPSK). However, advancements in digital technology now enable the processing of radio frequency (RF) signals within the digital time domain. This transition from analog to digital processing enhances demodulation accuracy, reduces noise susceptibility, and allows for more adaptive and reconfigurable receiver architectures. Digital demodulation techniques leverage high-speed signal processing algorithms and software-defined radio (SDR) platforms, facilitating seamless adaptation to various satellite communication standards without requiring extensive hardware modifications. The ability to implement advanced error correction codes and synchronization

algorithms further improves signal integrity and data recovery. Additionally, digital demodulators can efficiently handle wideband signals, supporting higher data rates essential for modern satellite applications such as Earth observation, remote sensing, and deep-space communications. The integration of field-programmable gate arrays (FPGAs) and application-specific integrated circuits (ASICs) in demodulator design enhances processing efficiency, enabling real-time adaptation to dynamic satellite link conditions. Furthermore, software-based implementations provide the flexibility to update modulation schemes and optimize performance remotely, reducing maintenance costs and operational complexity. As satellite communication continues to evolve, digital demodulation technologies play a crucial role in ensuring robust, scalable, and efficient data reception, ultimately enhancing the capabilities of ground stations to accommodate the growing demand for multi-satellite communication networks. Adjusted RF signals are carefully examined and after that demodulated continuously utilizing advanced flag handling procedures executed on FPGAs.

As a result of the use of FPGAs, the structure can have low power utilization, size and cost decrease. Moreover, these advanced demodulators can be reconfigured and moved up to upgrade the information rates in future. The BPSK/QPSK can be demodulating by various systems, for example, squaring loop, Costas loop and others in simple space. The Costas loop method has received for building up the demodulator in advanced space as in this the bearer recuperation and information demodulation should be possible all the while with square dimension plan.

The high information rate computerized demodulator is intended to perform IF intensification, sifting and simple to advanced change of the got IF flag pursued by a Digital demodulator. The fundamental plan system incorporates a configurable information rate BPSK/QPSK demodulation with COSTAS loop hardware using the adaptability of FPGA usage.

2 Theoretical Background

Costas loop is generally utilized in fields of radio innovation and has turned into a vital piece of correspondence frameworks, for example, satellite collector, radar and route frameworks. It has wide application on account of its extraordinary following execution [11-13]. A Costas loop essentially comprises of two multipliers called blenders, two low-pass filters (LPF) as arm filters, a low pass filter (LF), a phase detector (PD), a numerically controlled oscillator (NCO) and a 90 degree stage move. Fig.1 demonstrates the essential square graph of a Costas loop. The

information signals are sent to two multipliers of the upper branch brought in-stage part and the lower branch called quadrature segment. The in stage branch increases contribution by NCO's yield; the quadrature branch duplicates the contribution by NCO's yield after 90° stage move. The multiplier yields of the in-stage and quadrature branches are gone through low-pass filters, at that point duplicated together to get the blunder flag. The mistake flag is separated by the loop filter, whose yield is a control flag which controls the NCO's stage and recurrence.

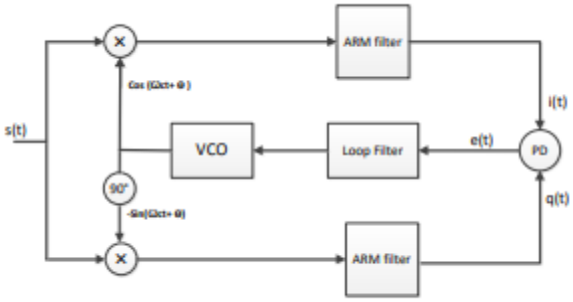

Fig.1 Block diagram of a basic Costas loop

3 Digital Implementation of Costas Loop Modules

In request to have an asset proficient usage, all Costas loop modules are planned so they would require the littlest measure of equipment assets. In fig.2 a square outline of the proposed Costas loop is delineated. In the accompanying passages these modules are portrayed in detail.

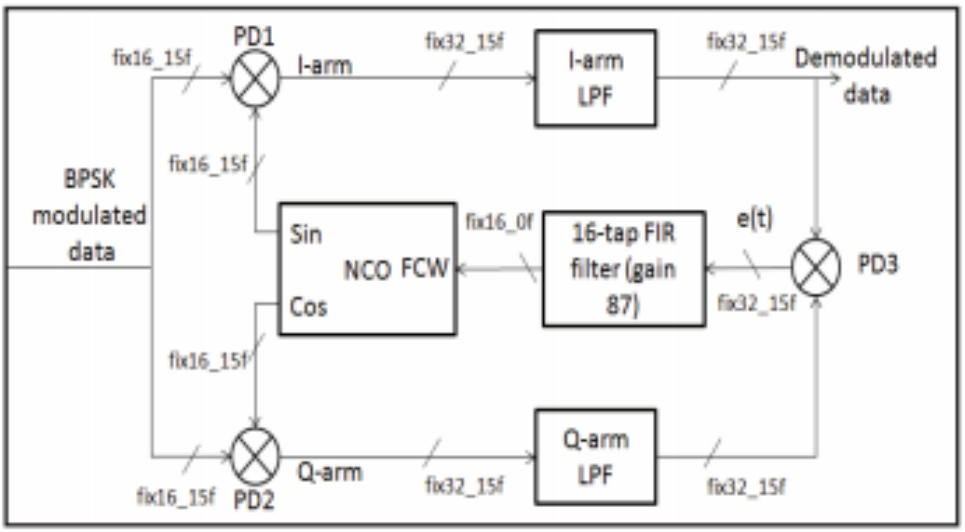

Fig. 2 Architecture of Costas Loop

The advanced execution engineering of the Costas loop is appeared in fig. 4. Settled point information type is utilized in the usage, 16-point accuracy for NCO yield and information, 32-

point exactness for filter activity. The BPSK regulated information is nourished to both the stage finders (PD's), the sine yield of the NCO is sustained to PD1 and cosine yield to PD2. A second request Butterworth filter would carry out the activity of the I-arm and Q-arm low pass filters. The mistake flag is produced by PD3 to which I-arm and Q-arm filters yield sustained in. The computerized loop filter is executed utilizing incorporate and dump filter, with legitimate gain parameters. The refined mistake motion from advanced loop filter gives the frequency control word (FCW) for the NCO. The demodulated information, free of stage and recurrence counterbalances, is inferred out of the I-arm filter while the Q-arm filter yield goes roughly zero.

3.1 AGC Module

In order to limit the noise bandwidth and also compensate the signal attenuation associated with the filter, an Automatic Gain Control has been designed. This AGC consist of a LPF, a level detector, a multiplier and a decimator. LPF limits the noise bandwidth; level detector determines the scaling factor for the multiplier; decimator down samples the input signal and reduces the sampling frequency to a value appropriate for the Costas loop. The input signals of this module are the I/Q branches resulted from the IF Mixer. AGC output signals are well suited for being processed by Costas loop. A block diagram of this AGC is depicted in fig.3 .

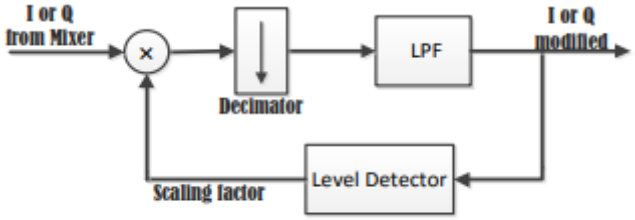

Fig.3 block diagram of the designed AGC

3.2 Numerically Controlled Oscillator (NCO)

A basic strategy for carefully creating an unpredictable or genuine esteemed sinusoid utilizes a query table plan. The query table stores tests of a sinusoid. An advanced integrator is then used to create an appropriate stage contention that is mapped by the query table to the coveted yield waveform. In [14], the creators execute NCO on a Xilinx FPGA in three sorts of ways, and the end that the strategy dependent on Xilinx ROM is better than the other two is procured. In this way, in this work, a Xilinx Block memory is utilized as the query table for the sinusoid tests. Fig.4 delineates the structured NCO. Both sine and cosine esteems are perused from the single ROM with the goal that the required number of the assets is diminished by a factor of 1/2 . With the end goal to have both sine and cosine esteems in the meantime, a ROM Address Controller

module is composed in VERILOG. This module works in a procedure with a quicker clock than the Costas loop process clock.

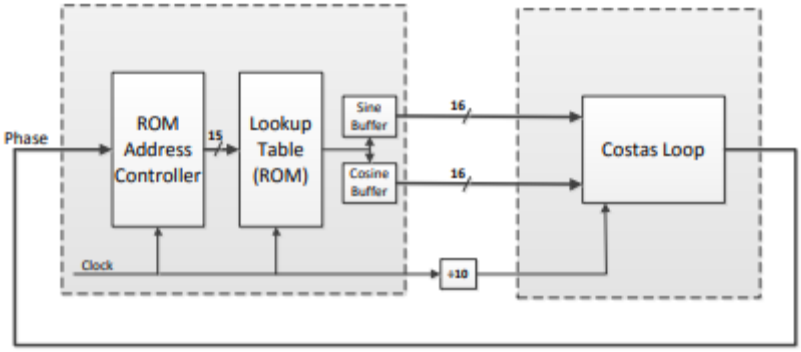

Fig.4 block diagram of a resource efficient NCO for Costas loop

3.3 ARM Filter

The arm filter transfer speed is a basic assignment to be tended to for structuring a demodulator. In this paper, cutoff recurrence of LPF is figured thinking about both Doppler recurrence and the image rate to expel the twofold recurrence segments. This filter is indistinguishable to the LPF which has been utilized in the transmitter as the beat shape filter. This filter is a first request Butterworth which expends less number of multipliers in contrast with a FIR filter and thus make the structure more asset and furthermore time effective.

3.4 Phase Detector (PD)

The principle capacity of a PD is to evaluate the stage distinction between the info flag and the NCO yield and deliver a mistake flag. For all-advanced Phase bolted loops, different stage finders like PFD (phase frequency identifier), EX– OR entryway, flip slump can be utilized [15]. Ina customary Costas loop stage identifier, genuine estimation of stage contrast is approximated by increase of arm signals which devours loads of equipment recourses. Circular segment digression stage locator is broadly utilized because of its high accuracy. It is demonstrated that the arctangent stage recognizing technique is the main strategy which can keep direct in the half (+90°) interim of information blunder go [15].

3.5 Loop Filter

The fundamental capacity of the loop filter is to change over the stage mistake to the recurrence deviation. In this work an advanced first request IIR filter has been intended for usage in FPGA. Square Diagram of this filter is delineated in fig.5

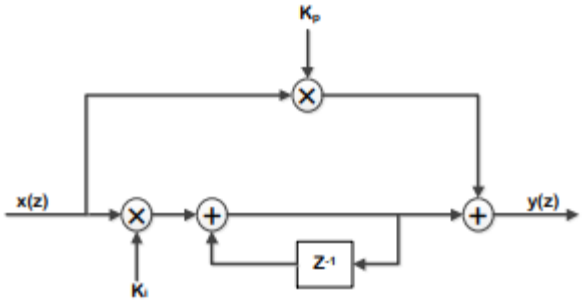

Fig.5 topology of the designed loop filter

4. Simulation Results

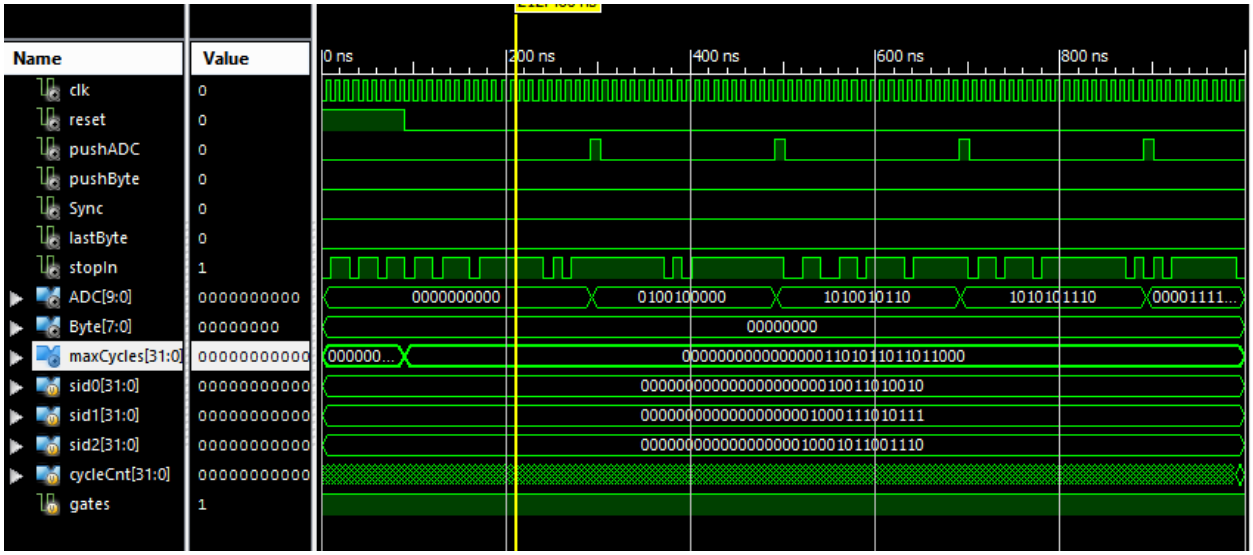

Fig. 6: Simulation output of the Costas loop

Device Utilization Summary (estimated values)			
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slices	4248	13312	31%
Number of Slice Flip Flops	794	26624	2%
Number of 4 input LUTs	8166	26624	30%
Number of bonded IOBs	6	221	2%
Number of MULT18X18s	30	32	93%
Number of GCLKs	2	8	25%

Fig. 7: Device Utilization Summary

5.Conclusion

In this paper an asset proficient all-advanced BPSK demodulator dependent on Costas loop was planned in XILINX and VERILOG. Distinctive modules of a traditional Costas loop, for example, NCO, Phase Detector, Loop filter and ARM filters were structured with the goal that they would devour the base measure of assets in a FPGA. Recreation results in XILINX and

furthermore Modelsim exhibit that the planned Costas loop is fit for recouping the information with stage and recurrence counterbalances as high as 20 percent of the examining recurrence and the required time for locking the information is lower than even an image time.

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