Optimized VLSI-Based Median Filter Design Using Data Comparator Logic for Real-Time Noise Reduction in Image Processing

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Abstract

Filters are essential for eliminating many kinds of noise from pictures, including Gaussian, random, and salt-and-pepper noises. Thus, in real-time applications, the hardware implementation of filters designed for Very Large-Scale Integration (VLSI) becomes crucial. However, issues with excessive look-up-table (LUT) usage, route delays, and power consumption plague conventional hardware-based filters. The use of a Median Filter (MF) using Data Comparator (DC) logic is the main focus of this study. The method starts with a data comparator controlled by multiplexer selection logic that determines the high and low values from a pair of numbers. The median value is then found by repeatedly applying the data comparator to nine-pixel combinations. The suggested MF-DC performs better than current methods in terms of noise reduction and hardware metrics like LUTs, latency, and power consumption, according to both subjective and objective assessments.

Keywords: Comparator, Median Filter, Data Comparator, LUT, Multiplexer, VIVADO, Noise Reduction, Real-Time Image Processing.

1. Introduction

Noise is undesirable information which degrades image quality.The image can be noisy because of dust present on the lens, electronic noise in camera, imperfection present in the image sensor or can be introduced when image data is transmitted over communication channel. The motive of image processing is to get rid of noise from a digital image while keeping its features unaltered. Image filter is the key blog of Image processing system. An impulsive noise can be added when image data transmitted over an insecure communication channel. It causes small size dots or dark/black spot on an image. Impulse noise is uniformly distributed and the most often mentioned noise in digital images. Further, Impulse noise can be divided into two parts. The first one is salt and pepper noise which is a type of impulse noise having noisy pixel intensity either 0 (minimum) or 255 (maximum) in the case of gray scale images. It appears as randomly scattered black or white dots over the images. The second one is the random-valued shot noise which has arbitrary valued noisy pixels. To remove these noises, it is necessary that the acquired image must pass through an image pre-processing stage defined as a filter. Spatial and frequency domain are two categories of the filtering operation. Generally, filters are implemented by MATLAB, OCTAVE software's in real time systems. As it is a well-known fact that software implementation offers less processing speed in comparison to hardware implementation. Hardware implementation has become better alternative after the boost in the VLSI technology. To reduce the power consumption in the systems, more cooling devices have to be incorporated results in the costly system. Keeping the same functional capabilities with the reduction in power factors are heavily demanding. Yet in that context, battery and power optimizing technology have not matured up to that target. Most of these products include embedded microprocessors, DSPs and ASICs. It is a provoking undertaking to accomplish low force plan of any VLSI circuit. There are various degrees of advancement in VLSI configuration measure for low force applications. For battery operated portable products, power has been the main concern. As System-on-Chip (SoC) developing with more power transistors, it requires less power consumption. Power consumption reduction in highly integrated SoC cut down the heating problem. It reduces the cost of expensive

packing and cooling mechanism. In this work, VLSI architecture for noise reduction in different imaging applications is proposed to deal with the above issues of power and cost reduction, respectively. To achieve low resources, this work mainly focusing on Verilog based coding mechanisms with FPGA prototype. Then, the subjective and objective image statistics are measured by using MATLAB environment. The major contributions of this work are as follows:

- Implementation of data comparator for identifying the high, low values using multiplexer selection logic.
- Implementation of multi-level network for selection of median value from nine pixels in a window.
- Implementation of MF-DC for removal of different types of noises from image using hybrid switching of data blocks.

2. Literature Survey

Nikitha, Mylaram, and Divya Gampala ,(2022)[1] focused on implementation of Hybrid Median Filter (HMF) using Data Comparator (DC) logic. Initially, the multiplexer selection logic-based data comparato r is used to identify the high and low values from two numbers. Then, data comparator is repeated for multiple number of times for nine pixels combinations, which identifies the median value from nine pixels. The subjective and objective evaluation shows that the proposed MF-DC resulted in superior performance in terms reduced noise, hardware metrics like LUTs, delay, and power consumption as compared to state of art approaches.Sanki, Pradyut Kumar, et al (2022)[2] proposed Real-Time Impulse Noise Removal (RTINR) algorithm and its hardware architecture are proposed for denoising images corrupted with fixed valued impulse noise. A decision-based algorithm is modified in the proposed RTINR algorithm where the corrupted pixel is first detected & is restored with median or previous pixel value depending on the number of corrupted pixels in the image. The proposed RTINR architecture has been designed to reduce the hardware complexity as it requires 21 comparators, 4 adders, and 2 line buffers which in turn improve the execution time. The proposed architecture results better in qualitative and quantitative performance in comparison to different denoising schemes while evaluated based on PSNR, IEF, MSE, EKI, SSIM,& FOM.Bevara, Vasudeva, Bevara Srinu, and Pradyut Kumar Sanki (2022)[3] proposed a new Decision Based Adaptive Denoising Filter (DBADF) algorithm & hardware architecture are proposed for restoring the digital image that is highly corrupted with impulse noise. The proposed DBADF detects only the corrupted pixels and that pixel is restored by the noise-free median value or previous value based upon the noise density in the image. The proposed DBADF uses a window initially and adaptively goes up to window based on the noise corruption more than 50% by impulse noise in the current processing window. G.LakshmiVara Prasad (2022)[4] focused on Information mining, data sets, ATM and correspondence exchanging, logical registering, booking, manmade brainpower, advanced mechanics, picture, video, and flag handling all require arranging. The proposed work fosters a clever information comparator to monetarily sort/rank request networks by speed, power, and region. This study presents a region productive Middle Channel Comparator. Priya, G. Karthigai, and D. Gracia Nirmala Rani (2022)[5] focused on the outbreak of COVID-19 challenged the existence of human life on earth. The diagnosis and treatment of this disease is highly crucial in current scenario. Since there is low difference in the intensity of normal cells and affected cells, Computed Tomography (CT) is an efficient tool for the diagnosis of lung infections caused due to COVID-19. In order to train a deep neural network, there is a requirement for huge number of labelled images. There is a necessity to develop an efficient neural network that requires less number of training images. To overcome these problems a novel network is developed for lung CT segmentation (SqueezeNet). For the extraction of energy values from the segmented image, Discrete Wavelet Transform (DWT) with lifting scheme is

incorporated in the framework. These energy values are used for training the classifier (ResNet).Sanki, Pradyut Kumar, and Rakesh Biswas (2022)[6] proposed that the Ultrasound images often get distorted by impulse noise during data acquisition and processing in the Back-end of the system, which overlay the finer details of the scanned body parts. Generally, a portable low-cost USG system doesn't have an impulse noise-cleaning module which hinders detections of smaller details in the images. A Depth Invariant Impulse Noise Removal (DIINoR) algorithm and its hardware architecture for real-time impulse noise removal from the corrupt USG image are proposed in this paper. In this decision-based algorithm, the corrupt pixel is first detected depending on the homogeneity of the processing window and is restored with the median of the window or previous pixel value. Testing of the DIINoR algorithm on different USG images establishes that the denoised images have superior quantitative performance compared to those of existing schemes Anbumani, V., et al(2022)[7] Based on a sorting network, the proposed approximate median filters (APMF) produce acceptable image quality on low-cost hardware. A specialized comparator is being developed to increase the noise-elimination capabilities of such filters. The inexact median filters (IMF) have a regular and modular architecture. Further, to reduce the power consumed by digital systems clock gating is employed. Clock with a View Into the Future Gating is a unique way of computing each FF's clock enabling signals one cycle ahead of time, based on the current cycle data of the FFs it depends on. The proposed filter is effective in terms of power, area, and speed, according to simulation findings. The filter's output quality is comparable to that of a precise filter, despite the trade- off between filtering precision and circuit features Mounika, G., and K. Vasanth (2022)[8] proposed on a 45nm based Data Comparator using different combinational style implementation is proposed. A Data comparator is a combinational circuit that uses a carry as reference to select greatest and smallest of two numbers. The proposed data comparator has carry generation unit implemented with a logic of subtraction using different combinational style such as decoder, multiplexer, basic subtractor logic etc. Kausar, Ahmad, and Rahul Shrivastava(2022)[9] proposed on the Image processing has many of the application in current scenario. During the image capturing or processing, some noise mix with the original image. Due to the noise issue the overall performance down or sometimes it failure. The images pixels mix with these types of the noise signal. There is various filters design which avoids or removes the noise signal. The advancement of the technology is going with the advance ICs processing. The VLSI architecture of filter design is useful in the FPGA ICs for the image processing applications. This paper reviews about the low-cost VLSI architecture of the filter for image denoising. Najafi, M. Hassan, et al (2018)[10] proposed that Sorting is a common task in a wide range of applications from signal and image processing to switching systems. For applications that require high performance, sorting is often performed in hardware with application-specified integrated circuits or field-programmable gate arrays. Hardware cost and power consumption are the dominant concerns. The usual approach is to wire up a network of compare-and-swap units in a configuration called the Batcher (or bitonic) network. Such networks can readily be pipelined. This paper proposes a novel area-efficient and power-efficient approach to sorting networks, based on "unary processing.". To mitigate the increased latency, this paper uses a novel time-encoding of data. The approach is validated with two implementations of an important application of sorting: median filtering. The result is a low cost, energy-efficient implementation of median filtering with only a slight accuracy loss, compared to conventional implementations. Srinu, Boni, Srinu Bevara, and M. Nagendra Kumar (2019)[11] proposed on the median filter with high throughput and good latency to suppress the impulse based noise on real time signal and image processing applications. It is partially affected by the median filter and its bias of the input stream is directly above the average of mathematical analysis. An efficient VLSI suitable hardware implementation of a median filter is presented, that uses compare and exchange unit. The proposed hardware structure reduces the hardware requirements and has a faster processing speed, when compared with some other existing techniquesAppiah, Obed,

Michael Asante, and James Benjamin Hayfron-Acquah(2021) [12] proposed method is based on the assumption that an image is available from the front (fully front). Skin areas were first detected using a color-based learning algorithm and six sigma techniques on RGB, HSV, and NTSC scales. Other analyzes involve morphological processing using the detection of the borderline and the detection of the reflection from the light source of the eye commonly referred to as the eye point. In the second step, a fast angle detection algorithm has been used to detect the placeholders on the face. The Fast Angle Finder works on the Angular Response Function (CRF) which is calculated as the minimum change in intensity in all possible directions. Finally, a comparison has been made with other filtering techniques based on the proposed protection techniques. This article has performed different experiments by using the IRIS Face Database.Balasamy, K., and D. Shamia(2021)[13] proposed algorithm focuses on developing an algorithm, which starts with pre-processing clinical image by Switched Mode Fuzzy Median Filter (SMFMF) for extracting the noise affected pixel thereby replacing the noisy pixel with the value of median pixel. Clinical image features, such as colour, shape, and texture, are extracted for selecting. Huang, Guangtan, et al (2021)[14] proposed on the Erratic noise often has high amplitudes and a non-Gaussian distribution. Least-squares–based approaches therefore are not optimal. This can be handled better with non–least-squares approaches, for example based on Huber norm which is computationally expensive. An alternative method has been published which involves transforming the data with erratic noise to pseudodata that have Gaussian distributed noise. It can then be attenuated using traditional least-squares approaches. This alternative method has previously been used in combination with a curvelet transform in an iterative scheme. In this paper, we introduce a median-filtering step in this iterative scheme. The median filter is applied following the slope direction of the seismic data to maximally preserve the energy of useful signals. The new method can suppress stronger erratic noise compared with the previous iterative method, and can better deal with random noise compared with the single-step implementation of the median filter. We apply the proposed robust denoising algorithm to a synthetic dataset and two field data examples and demonstrate its advantages over three different noise attenuation algorithms Shah, Anwar, et al(2021)[15] proposed method is used to refine the image quality and make it more informative. Many image-denoising algorithms had been proposed with their own pros and cons. This paper presents a comprehensive study of the median filter and its different variants to reduce or remove the impulse noise from gray scale images. These filters are compared with respect to their functionality, time complexity and relative performance.

3. Proposed Methodology

Commotion is signal-subordinate and is hard to be eliminated without disabling image subtleties. Various sorts of error influence the image, like Gaussian, drive, dot and Rician commotions. In the image denoising measure, data about the sort of error present in the original image assumes a huge part. The image error can be delegated either added substance or multiplicative. The image is a 2-D function f(x,y) of light intensities, where f is amplitude at any spatial coordinate x and y. The beam of light falls on an object and reflected light reaches to eyes. It makes human to see the object. The smallest element of the image is pixels. Each pixel represents intensity value at a particular location. Mathematically, image can be represented as Equation (1).

$$F(x,y) = I(x,y).R(x,y) \qquad (1)$$

Here, I (x,y) is intensity of incident light on object, R (x,y) is reflected light from object in intensity and F(x,y) is intensity of resultant image. The image restoration is the process to denoising a image, which has been distorted by prior knowledge of degradation model. Once the degradation model is known, by applying inverse process to recover the desired imagery. Image restoration is different than traditional image enhancement techniques. It is a subjective process, which produces more effective

results to an observer with and without using degradation model. The image degradation process is shown in Figure 1. image degradation model in the spatial domain is achieved by performing the convolution between f (x,y) and model function (h(x,y)).

$$F(x,y) = h(x,y) * f(x,y) + \eta(x,y) \quad (2)$$

Here, η (x,y) represents the speckle noise. Further, degradation model in the frequency domain is achieved by applying the Fourier transform as follows:

$$F(u,v) = h(u,v) * f(u,v) + \eta(u,v) \quad (3)$$

Here, u, v represents the frequency domain coefficients.

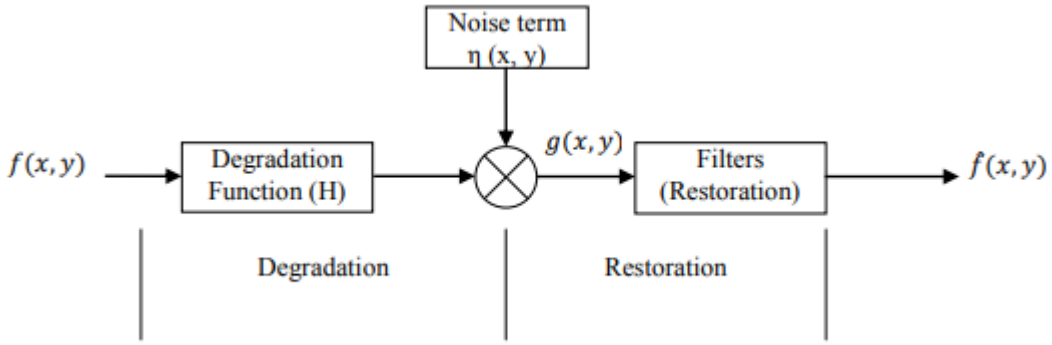


Figure 1. Image degradation model

The MF-DC is a digital non-linear method used to eliminate noise, like that of the medium filter. However, by keeping valuable details in the image, it typically does better than the mean filter. This filter class belongs to the class of filter that preserves the edge. These filters smooth down the data while maintaining the details. The median is only the average of all the pixel values in the area. It doesn't correspond to the mean (or average), but the median is half bigger and half smaller in the neighborhood. The median is a "center indication" stronger than the average. Like the medium, every pixel in the image is considered by the MF-DC and its close neighbors are examined to determine if it is typical of their surroundings. It replaces the median value with those values instead of just replacing the pixel value by the mean of the next pixel value. Particularly better than the typical filter is to take away impulsive noise. The MF-DC eliminates the noise as well as the fine details as the difference between them cannot be identified. Anything that is comparatively tiny in size with the area size will minimize and filter out the median value. In other words, the MF-DC can differentiate between fine detail and noise.

3.1 Data comparator

Figure 2 shows the block diagram of data comparator, which is used to perform the selection of highest and lowest values from the given two input data. Further, the data comparator block contains inputs as A, B and outputs are High (H) and Low (L).

Step 1: Initially, A < B condition is verified, if condition is satisfied selection line of multiplexer becomes one, else condition failed selection line becomes zero.

Step 2: Input-A is applied as Data-input-0 and Input-B is applied as Data-input-1 to 2to1 multiplexer. If A value is smaller than B, then selection line becomes one and multiplexer generates

H as input-B through selection switching. If A value is higher than B, then selection line becomes zero and multiplexer generates H as input-A through selection switching.

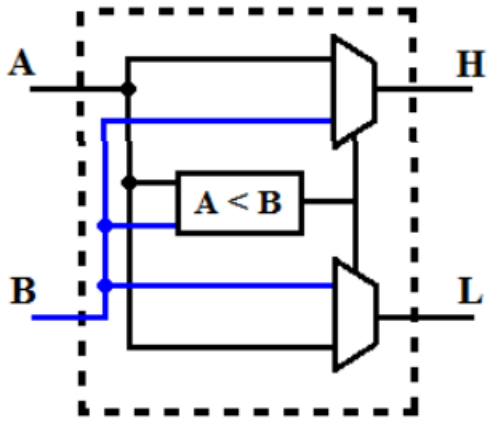


Figure 2. Block diagram of data comparator.

Step 3: Input-B is applied as Data-input-0 and Input-A is applied as Data-input-1 to 2 to1 multiplexer. If A value is smaller than B, then selection line becomes one and multiplexer generates L as input-A through selection switching. If A value is higher than B, then selection line becomes zero and multiplexer generates L as input-B through selection switching.

Hardware architecture of MF

Figure 3 shows the hardware architecture of MF-DC, which contains the fourteen number of hardware resource blocks. Here, inputs P0, P1, P2, P3, P4, P5, P6, P7, and P8 are applied to MF-DC, which generates the median value as M. Here, DC-1, DC-2, DC-3 are grouped together and performs the selection of high (H1), low (L1) and median (M1) values. Similarly, DC-6, DC-7, DC-8 and DC-15, DC-16, DC-17 performs the generation of high, low and median values. Further, DC-4 is used to select the lowest value from H1, H2, H3 outcomes. Furthermore, DC-18 is used to select the highest value from L1, L2, L3 outcomes. Similarly, DC-9, DC-10, DC-11 are grouped together and performs the selection of high, low and median values. Like this, the process will continue and generates the median value (M) from DC-14 low outcome.

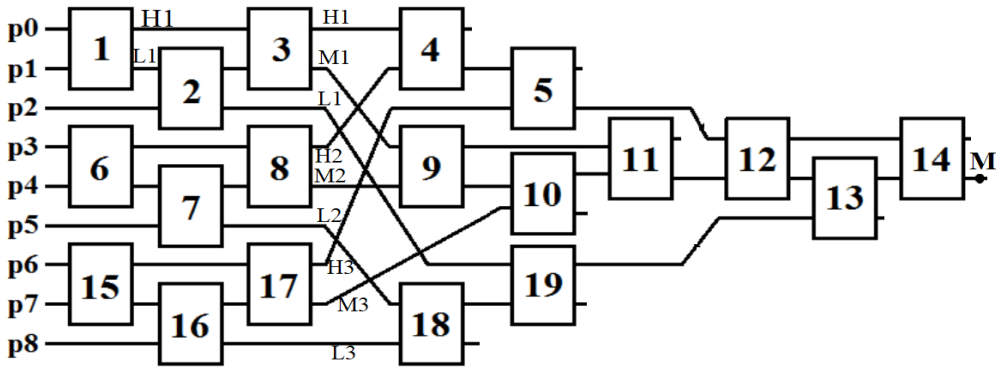


Figure 3. Hardware architecture of MF-DC.

Figure 4 provides a numerical example that might help better illustrate how the MF-DC system works. In this case, the median value is defined by the two non-median outputs that are located the closest to it. As can be seen in this diagram, the H1, H2, and H3 blocks are used to sort the four

highest pixel values (95, 92, 90, and 75), which results in 75 being the upper range. At the same time, the three lower ranges (L1, L2, and L3) are used to sort the four lowest values (10, 20, and 50), which results in 53 being the lower range.

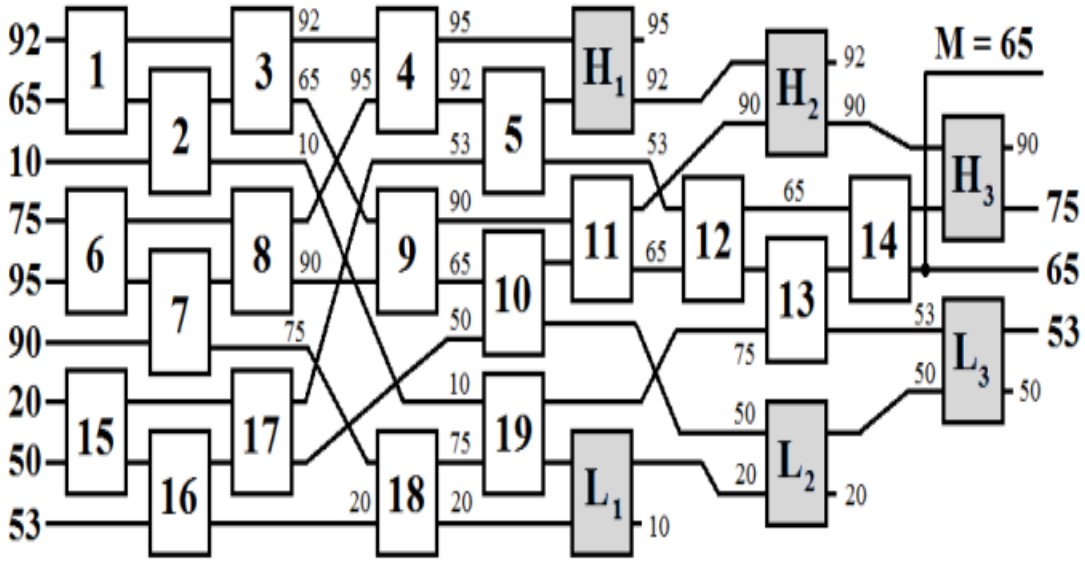


Figure 4. Example of MF-DC.

4. Results and Discussion

Vivado software was used to create all the MF-DC designs. This software programmed gives two types of outputs: simulation and synthesis. The simulation results provide a thorough examination of the MF-DC architecture in terms of input and output byte level combinations. Decoding procedure approximated simply by applying numerous combinations of inputs and monitoring various outputs through simulated study of encoding correctness. The use of area in relation to the LUT count will be accomplished because of the synthesis findings. In addition, a time summary will be obtained about various path delays, and a power summary will be prepared utilizing the static and dynamic power consumption. Further, MatlabR2016a software is used to evaluate the subjective performance of MF-DC.

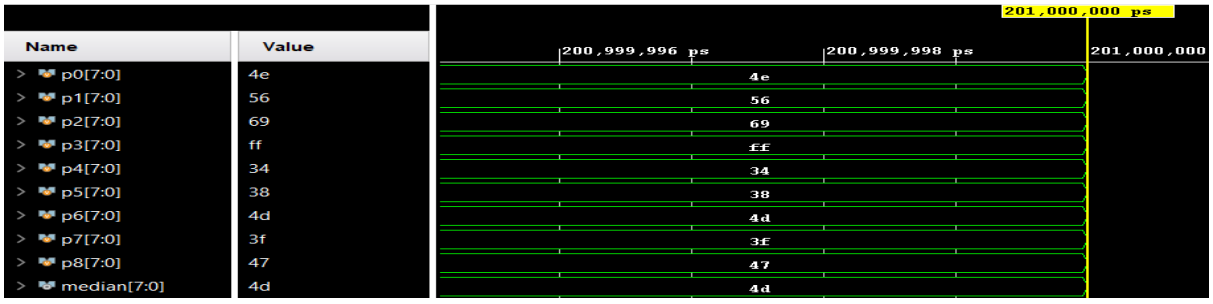
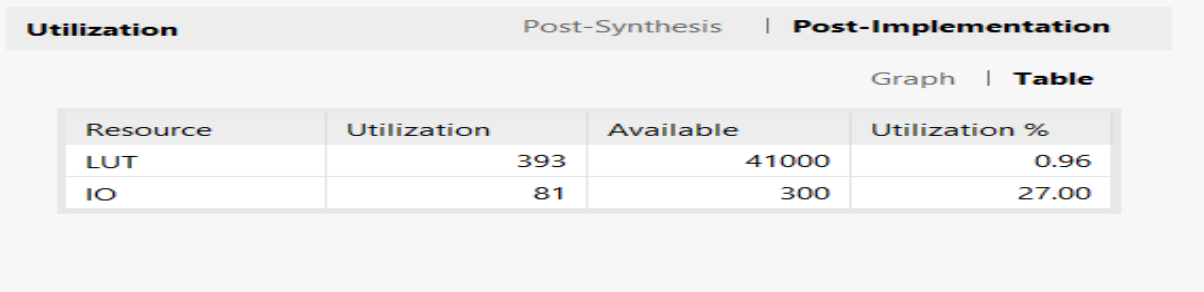


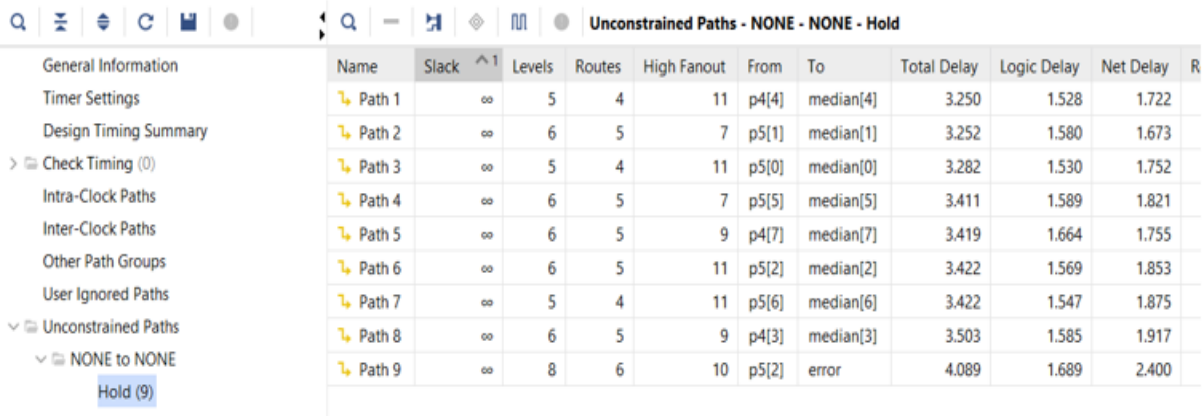
Figure 5 Simulation outcome of MF-DC

Figure 5 presents the simulation outcome of MF-DC. Here, P0, P1, P2, P3, P4, P5, P6, P7, P8 are the inputs to MF-DC and median is the output value. Figure 6 shows the design (area) summary of proposed method. Here, the proposed method utilizes the low area in terms of slice LUTs i.e., 437 out of available 303600. Figure 7 shows the time summary of proposed method. Here, the proposed method consumed total 20.375ns of time delay, where 1.726ns is logical delay, and 18.649ns is route delay. Figure 6.4 shows the power consumption report of proposed DCM-RTPG-BFD. Here, the proposed DCM-RTPG-BFD consumed power as 32.83 milli watts.



Resource	Utilization	Available	Utilization %
LUT	393	41000	0.96
IO	81	300	27.00

Figure 6. Design summary.



Name	Slack	Levels	Routes	High Fanout	From	To	Total Delay	Logic Delay	Net Delay
Path 1	∞	5	4	11	p4[4]	median[4]	3.250	1.528	1.722
Path 2	∞	6	5	7	p5[1]	median[1]	3.252	1.580	1.673
Path 3	∞	5	4	11	p5[0]	median[0]	3.282	1.530	1.752
Path 4	∞	6	5	7	p5[5]	median[5]	3.411	1.589	1.821
Path 5	∞	6	5	9	p4[7]	median[7]	3.419	1.664	1.755
Path 6	∞	6	5	11	p5[2]	median[2]	3.422	1.569	1.853
Path 7	∞	5	4	11	p5[6]	median[6]	3.422	1.547	1.875
Path 8	∞	6	5	9	p4[3]	median[3]	3.503	1.585	1.917
Path 9	∞	8	6	10	p5[2]	error	4.089	1.689	2.400

Figure 7. Time summary.

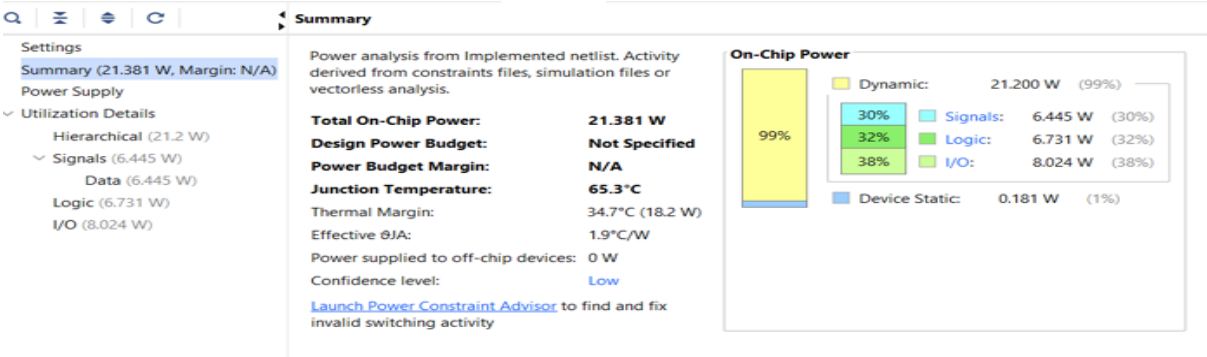


Figure 8. Power summary.

Figure 9 shows the filtering performance of various methods like SMF [11], DMF [12], AMF [13], and proposed MF-DC. Here, SMF [11] and AMF [13] methods resulted outcome still contains the high her noises, DMF [21] method outcome contains the low-level noises. But the proposed MF-DC method resulted outcome is looks like the original image. Table 1 compares the performance evaluation of proposed MF-DC method. Here, the proposed MF-DC resulted in superior (reduced) hardware performance in terms of LUTs, time-delay, and power consumption as compared to conventional approaches such as SMF [11], DMF [12], and AMF [13]. Further, the proposed MF-DC resulted in improved subjective performance in terms of peak signal to noise ratio (PSNR), stature similarity index metric (SSIM) as compared to conventional approaches such as SMF [11], DMF [12], and AMF [13]. Further, the graphical representation of performance comparison is presented in Figure 9.

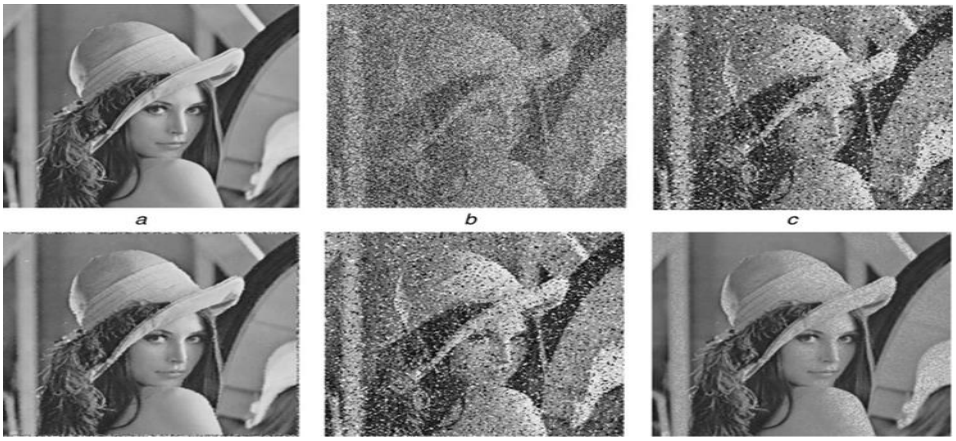


Figure 9. Visual performance of MF-DC. (a) original image, (b) noisy image, (c) SMF [11], (d) DMF [12], (e) AMF [13], (d) proposed MF-DC.

Table 1. Performance evaluation.

Metric	SMF [11]	DMF [12]	AMF [13]	Proposed MF-DC
LUTs	767	655	542	393
Time delay (ns)	51.927	43.837	32.735	3.58
Power consumption (mw)	82.61	73.41	58.26	21.200
PSNR (dB)	37.34	42.45	48.38	54.53
SSIM	0.827	0.893	0.927	0.992

5.Conclusion

The development of a Median Filter by making use of Data Comparator logic is the primary emphasis of this study. In the beginning, a multiplexer selection logic-based data comparator is used in order to determine which of two numbers have high and low values. After then, the data comparator is carried out several times for the nine different possible combinations of pixels, which determines the median value for all nine of those values. The subjective and objective evaluations both reveal that the suggested MF-DC resulted in greater performance when compared to the state-of-the-art techniques in terms of decreased noise, latency, and power consumption. Hardware metrics such as LUTs were also reduced and software metrics such as PSNR, SSIM are improved using the proposed MF-DC approach. Further, this work can be extended with the hybrid adaptive filters for improved PSNR performance.

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