Design of Quantum-Dot Cellular Automata-Based Shift Register Circuit using D-Flip Flop

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ABSTRACT

With the rising adoption of quantum-dot cellular automata (QCA) nanotechnology, nanoscale digital circuits offer numerous advantages over traditional CMOS devices, such as lower power consumption, enhanced processing speed, and higher density. Various flip-flop designs have been proposed in the literature for implementation using QCA technology. However, many of these designs face challenges such as high cell counts, significant area usage, and latency, resulting in increased circuit costs. To address these issues, this work surveys existing literature on D flip-flop (DFF) designs and the complex sequential circuits that can be constructed from them. A new Shift Register design was proposed in this study. To evaluate its performance, an extensive comparison with existing QCA designs was conducted.

This paper presents an optimized design for sequential circuits, such as shift registers using majority gates and implementing a cell minimization technique. This approach aims to reduce both the area and complexity of the circuits.

The design and validation of these blocks are supported by specialized software such as QCADesigner, purposely designed for QCA circuit design and analysis. These tools provide accurate modeling and simulation, ensuring the reliability and functionality of proposed designs.

Keyword : Quantum-Dot Cellular Automata, Sequential Circuit, Shift Register, D Flip-Flop.

1. INTRODUCTION

The evolution of electronic circuits in response to market demands has spurred the development of several nanoscale technologies like CNFET, FinFET, and Quantum-dot Cellular Automata (QCA) in recent decades. These innovations aim to meet the increasing need for smaller sizes, faster speeds, and enhanced efficiency in electronic devices. Nonetheless, the transition to nanoscale transistors has introduced challenges, including leakage current and heightened energy consumption due to quantum effects.

QCA technology, as emphasized in the International Technology Roadmap for Semiconductors study, presents a promising solution to these challenges. It offers a fresh computational paradigm with the potential to enable nano-computers to operate at terahertz (THz) level rates. General-purpose gates like

multiplexers and XOR gates have garnered significant interest from researchers due to their ability to streamline circuit complexity and lower costs.

Given this context, enhancing these gates is crucial for boosting the performance of circuits that rely on them. This study introduces a novel architecture for the XOR block in QCA format. Unlike traditional XOR gates, the proposed structure offers dual functionality, supporting both 2-input and 3-input XOR operations. This adaptability enables the block to seamlessly integrate into various circuits, thereby enhancing flexibility and adaptability in circuit design.

2. QCA BACKGROUND

The foundation of QCA technology lies in the principle of electron repulsion, where the basic unit is a small cell typically represented in a specific shape (refer to Figure 1).

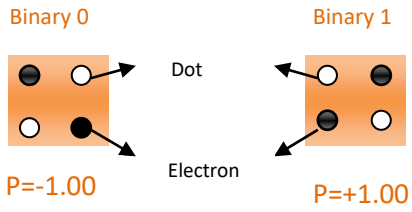

Figure 1 QCA Cell Configuration.

By arranging specific groups of these cells, logic gates can be constructed [13]. Among these gates, the majority gate (illustrated in Figure 2) serves as a fundamental building block from which other gates can be derived. Researchers have dedicated attention to this pivotal block, examining its reliability, applications, and complexity across various input configurations [03–12].

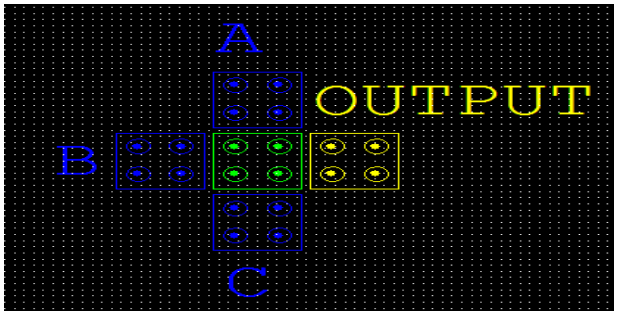

Figure 2. Cell Configuration of Majority block

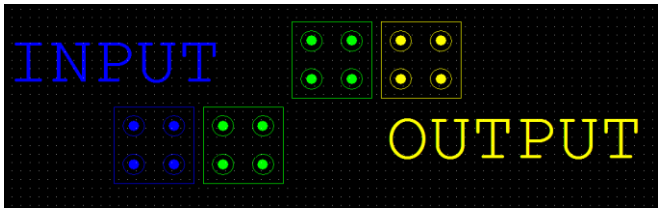

Figure 3.Cell Configuration of Inverter block

In addition to the majority gate, another essential component for QCA circuits is the inverter block (Figure 3), necessary to complete all required functions. Interconnections between circuit blocks are facilitated by QCA-wire, which comprises a chain of cells (as depicted in Figure 4) [2,14].

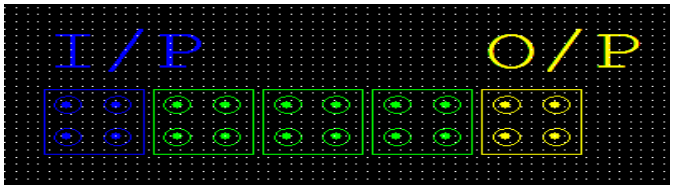

Figure 4.Configuration of QCA wire

Furthermore, ensuring proper data flow control and synchronization is vital, achieved through the provision of a clock signal. This signal governs the timing of data movement, ensuring accurate and synchronized results. In instances where QCA circuits involve a significant number of cells, they can be divided into zones, each characterized by four clock transitions: Relax–Switch, Switch–Hold,

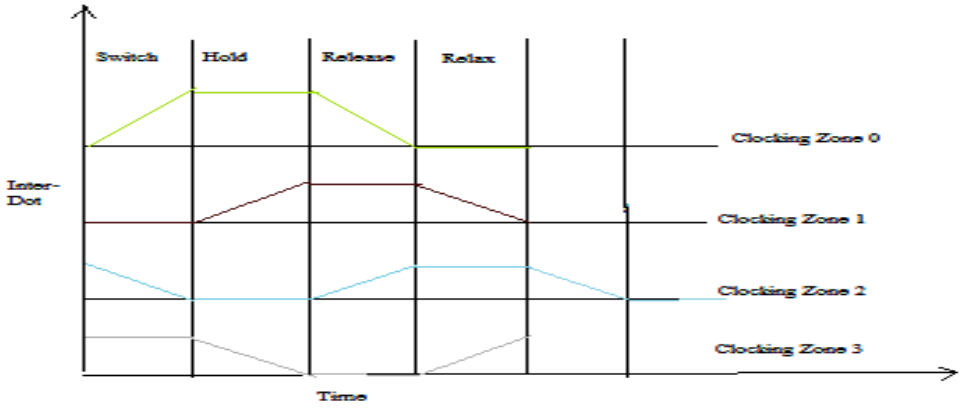

Figure 5. QCA Clocking with 4-Phases

[add any other necessary transitions here]. Hold–Release, Release–Relax) [1]. Figure 5 represents the clock signal that is commonly used in QCA technology.

D Flip-Flop

A flip-flop is a single-bit storage device and a type of sequential circuit. Its output depends on both the current input and the previous output.

Table 1 Characteristic Table of D Flip-Flop

Q	D	Q_{t+1}
0	0	0
0	1	1
1	0	0
1	1	1

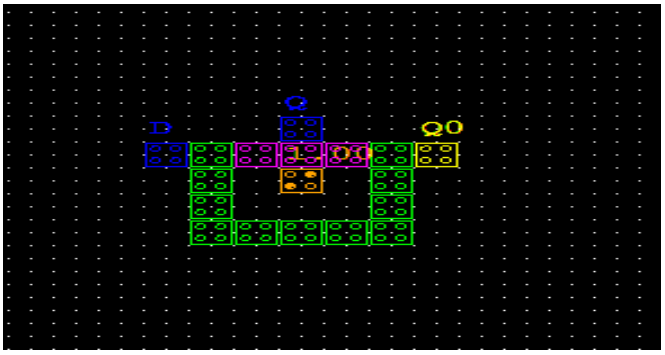

Figure 7. QCA Cell Layout of D-FF

3. CELL MINIMIZATION TECHNIQUE

The proposed design uses a cell minimization technique to reduce the number of majority gates without adding extra cells. This approach aligns the majority gates in parallel to shorten the circuit length. Furthermore, the output and polarization are directly incorporated into the majority gates, eliminating the need for additional cells.

4. PROPOSED DESIGN OF SHIFT REGISTERS

A shift register is a type of digital memory device. Bits are input at one end of the shift register and exit from the other end, referred to as the left and right ends. Therefore, the shift register operates as a bidirectional FIFO (First In, First Out) circuit. It is frequently utilized in converters that translate parallel data to serial data or vice versa. Additionally, it can function as a delay circuit and as a digital pulse encoder.

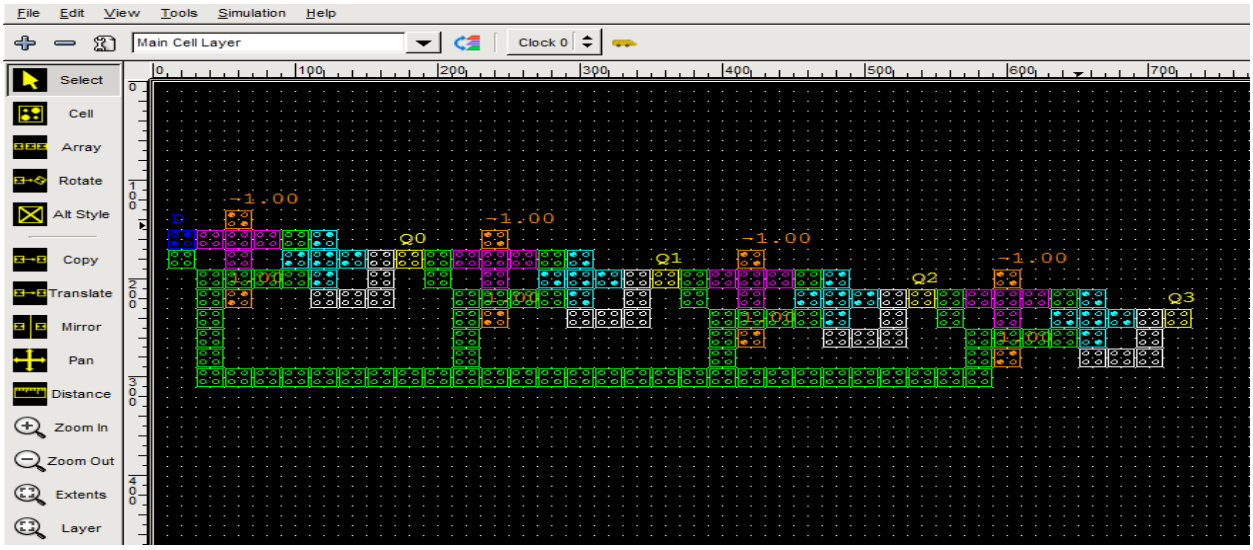

Figure 6. Proposed QCA Cell Layout of Shift Register by using D-FF

A shift register is a series of flip-flops that share a common clock signal, with the output of each flip-flop connected to the data input of the next flip-flop in the sequence. Since a shift register can operate in multiple dimensions, it is often implemented by running several shift registers of the same bit length in parallel.

5. SIMULATION RESULTS

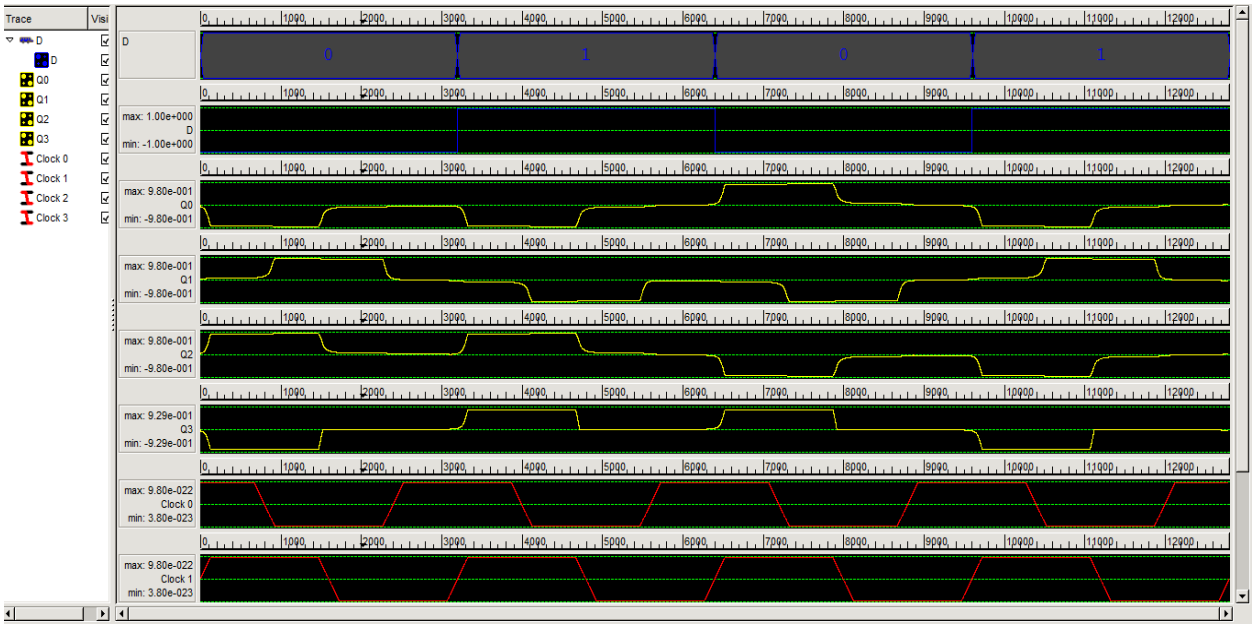

Figure 7. Simulation Result of Shift Register

Table 2 Performance Comparison

S.No.	Parameter	Existing Work	Proposed work
1.	Cell count	138	134
2.	Area	0.14 μm^2	0.019 μm^2
3.	Latency	4	0.75
4.	Quantum cost	138	134

6. CONCLUSION

In this work, efficient QCA structures for Shif-Register is proposed, simulated and evaluated. The structures, based on a D Flip-Flop. The sequential circuit is designed with reduced complexity, making them shift register designs. The QCA layout designs feature a minimal cell count and area, resulting in an optimal design. The functionality of shift registers has been verified using QCADesigner 2.0.3.

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